LONWORKS®

FTT-10A Free Topology Transceiver User's Guide

Version 6

ECHELON®
Corporation

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Echelon Corporation
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Introduction

The FTT-10A Free Topology Twisted Pair Transceiver provides a simple, cost-effective method of adding a LONWORKS transceiver to any Neuron® Chip-based control system. A replacement for the popular FTT-10 transceiver, the FTT-10A transceiver supports polarity insensitive, free topology wiring, freeing the system installer from the need to wire using a bus topology (differences between the FTT-10A and FTT-10 transceivers are described in Appendix A). Star, bus, and loop wiring are all supported by this architecture. Free topology wiring reduces the time and expense of system installation by allowing the wiring to be installed in the most expeditious manner. It also simplifies network expansion by eliminating restrictions on wire routing, splicing, and node placement.

The FTT-10A transceiver consists of an isolation transformer that is integrated with a 78kbps differential Manchester coded communication transceiver. Pins are provided for connections to the Neuron Chip Communications Port (CP) and clock lines, +5V power, and the twisted pair network. The FTT-10A transceiver provides automatic detection of the input clock frequency at 5, 10, and 20MHz. The pins are keyed to prevent accidental reversal during mounting. The FTT-10A transceiver appears as a high impedance to the network when unpowered, and does not interfere with network communications when powered down.

The transceiver is housed in an encapsulated plastic shell which contains the transformer and signal processing electronics. The compact package is only 7.2mm (0.28 inches) high and is ideal for use in low profile applications such as DIN packs. The sealed housing protects the transceiver should conformal coating or other forms of environmental sealing be required on the printed circuit assembly.

The FTT-10A transceiver is compatible with Echelon's LPT-10 Link Power Transceiver, and these transceivers can communicate with each other on a single twisted pair cable. This capability provides an inexpensive means of interfacing to nodes whose current or voltage requirements would otherwise exceed the capacity of the link power segment. When equipped with an FTT-10A transceiver, these nodes can be operated from a local power supply without the need for additional electrical isolation from the link power network.

The FTT-10A transceiver also provides electrical isolation for I/O devices that are grounded, allowing such devices to be used on a link power network segment. In many applications, some I/O devices are grounded, either to meet functional requirements or safety regulations. The transformer of the FTT-10A transceiver electrically isolates the node from the segment, allowing devices connected to the node to be grounded without impairing communications.

A twisted pair channel may be comprised of multiple segments separated by a physical layer repeater. A physical layer repeater permits a twisted pair network to grow inexpensively to encompass many more nodes or longer wire distances than would otherwise be possible. The FTT-10A transceiver includes a physical layer repeater feature that allows LonTalk® data to be exchanged between network segments by interconnecting two or more FTT-10A transceivers.

Using the FTT-10A transceiver can save literally thousands of hours of development time compared with a custom-designed transceiver. The transceiver is designed to comply with both FCC and EN 55022 EMI requirements, minimizing time consuming and expensive testing. As a U.L. Recognized component, the FTT-10A transceiver can be integrated into a product without further safety testing. The transceiver is small enough to fit into virtually any application, and is economically priced for OEM applications of any volume.

Applications

A conventional control system using bus topology wiring (such as RS-485) consists of a network of sensors and control outputs that are interconnected using a shielded twisted wire pair. In accordance with RS-485 guidelines, all of the devices must be wired in a bus topology to limit electrical reflections and ensure reliable communications. There is a high cost associated with installing and maintaining the cable plant that links together the many elements of an RS-485-based control system. Bus topology wiring is more time consuming and expensive to install because the installer is unable to branch or star the wiring where convenient: all devices must be connected directly to the main bus.

The best solution for reducing installation and maintenance costs and simplifying system modifications is a free topology communication system. Echelon's free topology transceiver (FTT) technology offers just such a solution, and provides an elegant and inexpensive method of interconnecting the different elements of a distributed control system.

A free topology architecture allows the user to wire the control devices with virtually no topology restrictions. Power is supplied by a local +5VDC power supply located at each node (figure 1.1).

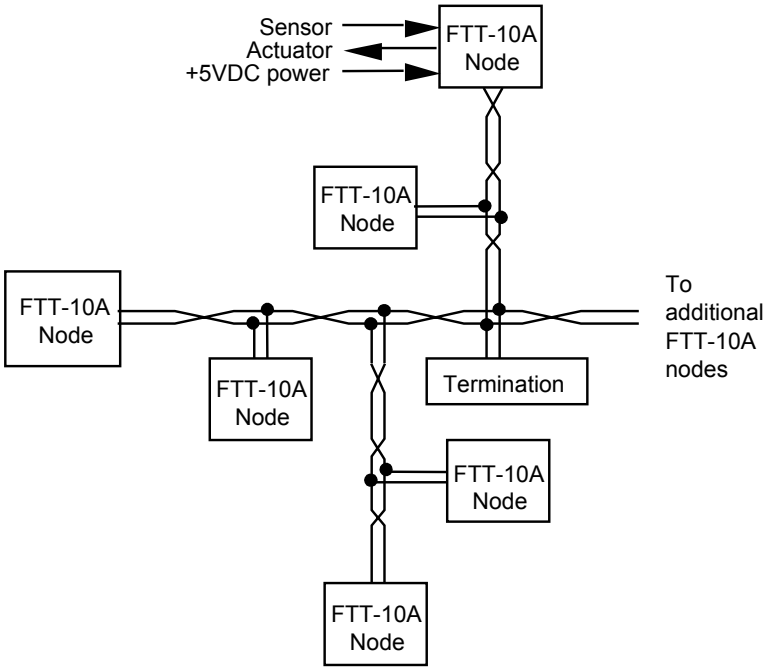


Figure 1.1 Free Topology Transceiver System

Unlike bus wiring designs, the FTT-10A system uses a free topology wiring scheme that supports star, loop, and/or bus wiring (figure 1.2). This design has many

advantages. First, the installer is free to select the method of wiring that best suits the installation, reducing the need for advanced planning and allowing last minute changes at the installation site. Second, if installers have been trained to use one style of wiring for all installations, free topology technology can be introduced without requiring retraining. Third, retrofit installations with existing wiring plants can be accommodated with minimal, if any, rewiring. This capability ensures that FTT-10A technology can be adapted to both old and new projects, widening the potential market for FTT-10A-based products. Finally, free topology permits FTT-10A systems to be expanded in the future by simply tapping into the existing wiring where it is most convenient to do so. This reduces the time and expense of system expansion, and from the customer's perspective, keeps down the life cycle cost of the free topology network.

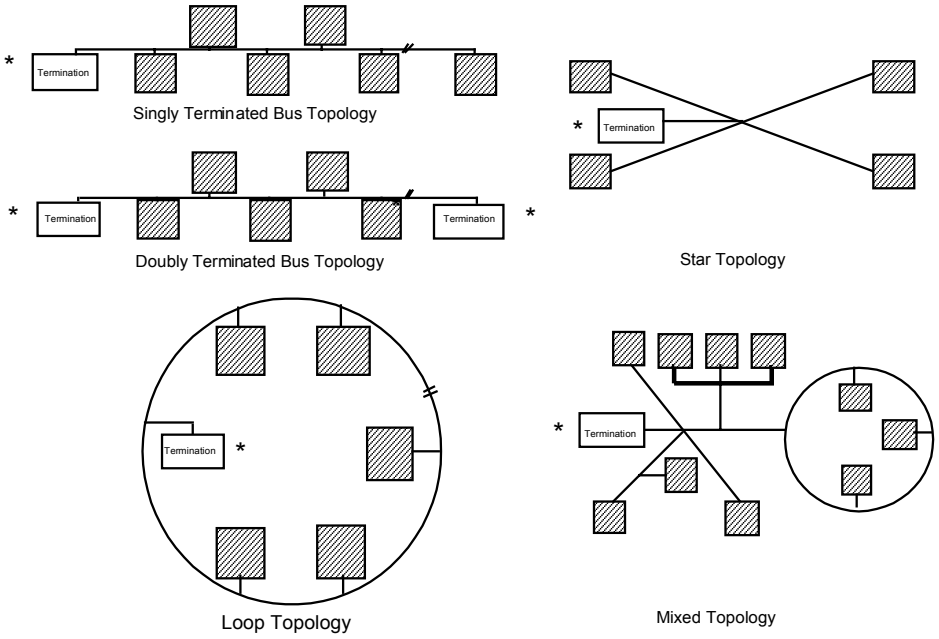
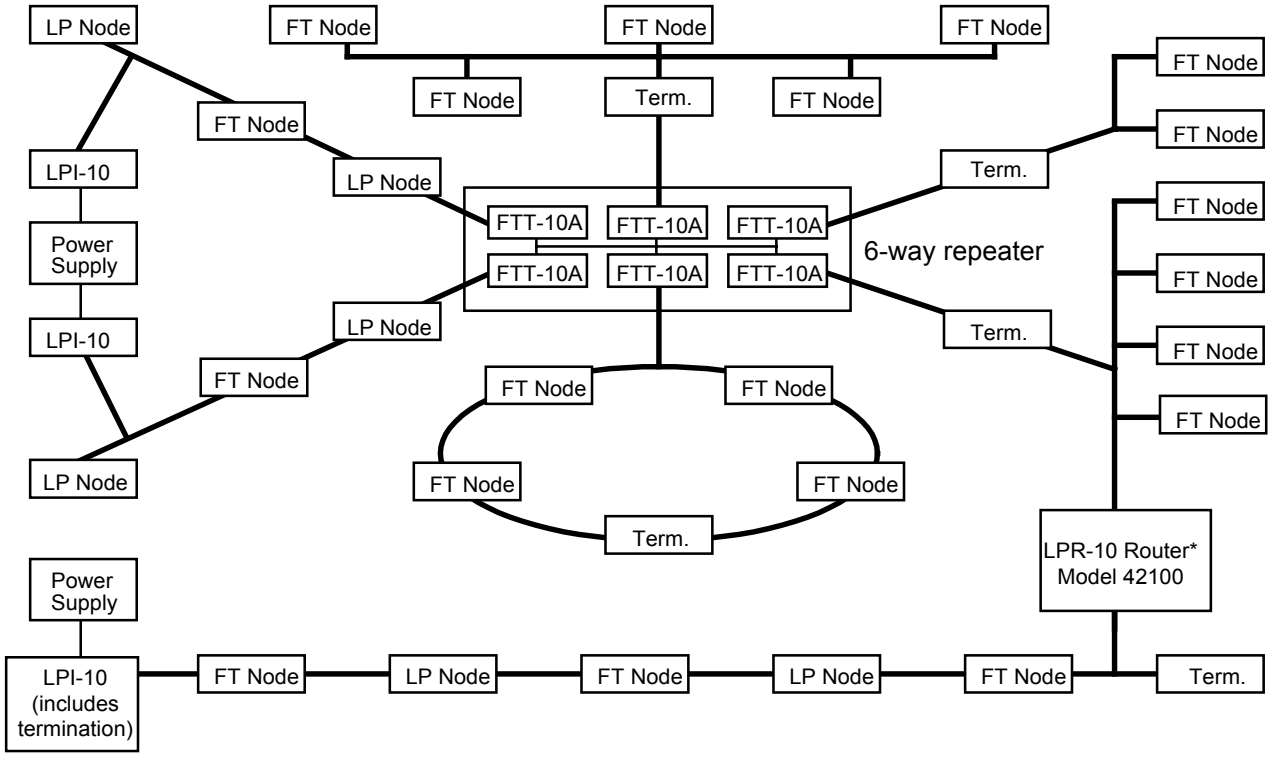


Figure 1.2 Typical Wiring Topologies Supported by the FTT-10A System
(* The actual termination circuit will vary by application.)

System expansion is simplified in another important way, too. Each FTT-10A transceiver incorporates a repeater function. If a network segment grows beyond the maximum number of transceivers or total wire distance, then additional FTT-10A segments can be added by interconnecting transceivers using the repeater function (figure 1.3). The repeaters will transfer LonTalk data between the two segments, doubling the number of transceivers as well as the length of wire over which they communicate. The repeater function permits an FTT-10A network to grow as system needs expand, without retrofitting existing controllers or requiring the use of specialized bridges. Note that only one repeater should be in series between any two nodes on a channel. Systems with high levels of network traffic may benefit from the



use of LONWORKS routers, such as Echelon's LPR-10, which forward packets only when necessary.

*A router must be used in this location because it is not permissable to have two repeaters in series on a channel.

Figure 1.3 Free Topology Channel Illustrating FTT-10A and LPT-10 Transceiver Compatibility and Network Expansion Using Physical Layer Repeaters (Repeaters simplified for illustration purposes)

Audience

The *LONWORKS FTT-10A Free Topology Transceiver User's Guide* provides specifications and user instructions for FTT-10A transceiver customers and users of control modules, network interfaces, and routers based on the FTT-10A transceiver.

Content

This manual provides detailed technical specifications on the electrical and mechanical interfaces and operating environment characteristics for the transceiver module.

This document also provides guidelines for migrating applications from a LonBuilder Developer's Workbench Emulator or NodeBuilder Development Tool to an FTT-10A-based node. Complete references and vendor sources are included to simplify the task of integrating the transceiver with application electronics.

This document has a list of references in Chapter 7. Whenever a reference document is addressed, a superscript number corresponding to the reference has been placed in

the text, e.g., Standler[10]. Whenever a specific chapter or section within a reference has been referred to, the reference is enclosed in brackets and the chapter is addressed by number, e.g., Reference [1], Chapter 7.

Related Documentation

The following Echelon documents are suggested reading:

LonBuilder User's Guide (078-0001-01)

NodeBuilder User's Guide (078-0141-01)

Neuron C Programmer's Guide (078-0002-01)

LonBuilder Startup and Hardware Guide (078-0003-01)

LONMARK™ Layers 1-6 Interoperability Guidelines (078-0014-01)

LONMARK™ Application Layer Interoperability Guidelines (078-0120-01)

Neuron Chip Data Book (published by Toshiba and Cypress)

LONWORKS FTT-10A Free Topology Transceiver data sheet (003-0111-01)

LONWORKS Custom Node Development engineering bulletin (005-0024-01)

LPI-10 Link Power Interface Module User's Guide (078-0104-01)

LPT-10 Link Power Transceiver User's Guide (078-0105-01)

Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks engineering bulletin (005-0023-01)

2

Electrical Interface

The FTT-10A Free Topology Transceiver provides a polarity insensitive connection to the twisted pair network, an interface to the Neuron Chip communications port, and a physical layer repeater function for expanding the size of a network.

Transceiver Pinout

The pinout of the FTT-10A transceiver is shown in table 2.1. Table 2.2 lists the electrical specifications of the FTT-10A transceiver. All specifications apply over the full operating temperature and supply voltage ranges unless otherwise noted.

Table 2.1 FTT-10A Transceiver Pinout

Name	*Pin*	*Type*	*Function*
VCC	1		5V DC input
NET_B	2		Network port, polarity insensitive
NET_A	3		Network port, polarity insensitive
RXD	4	CMOS digital output capable of driving one Neuron Chip and one HC-type input	Neuron Chip CP0
TXD	5	CMOS digital input with tri-state detection	Neuron Chip CP1
CLK	6	Digital input, CMOS level	Transceiver clock input from Neuron Chip's CLK2
T1	7	Bidirectional analog	Used for ESD clamping & transient protection
GND	8		Ground
T2	9	Bidirectional analog	Used for ESD clamping & transient protection

Table 2.2 FTT-10A Transceiver Electrical Specifications

Parameter	*Min*	*Typ*	*Max*	*Units*
Operating temperature range	-40		+85	degrees C
V_{CC} input supply voltage	4.75	5	5.25	Volts
V_{CC} input supply current receive transmit			 5 20	mA
DC resistance between NET_A and NET_B			20	Ω
Transmitter raised cosine waveform peak-to-peak amplitude into 52.3 Ω network termination		1.35		Volts

The preferred interconnection between the FTT-10A transceiver and a Neuron Chip is shown in figure 2.1. This schematic has been tested for ESD under both the preferred contact-discharge method and the alternate air-discharge method for electrostatic discharge (ESD). It exceeds level 4 in accordance with EN 61000-4, and **is recommended for all standard applications.** (See Chapter 5 for more details about EN 61000-4). **If the ESD protection requirements for the application are undefined or unknown, then the circuit shown in figure 2.1 or 2.2 should be used.**

Figure 2.1 is not a complete schematic, since the clock, reset and power supply bypass circuits will vary depending on the Neuron Chip type and application. For complete Neuron Chip application schematics and information, refer to the *Neuron Chip Databook*[2,3]. See Chapter 3 for mechanical specifications and printed circuit board (PCB) footprint information. **See Chapter 5 (1000-4-6 testing) to determine if a network isolation common-mode choke is required for EMC compliance.**

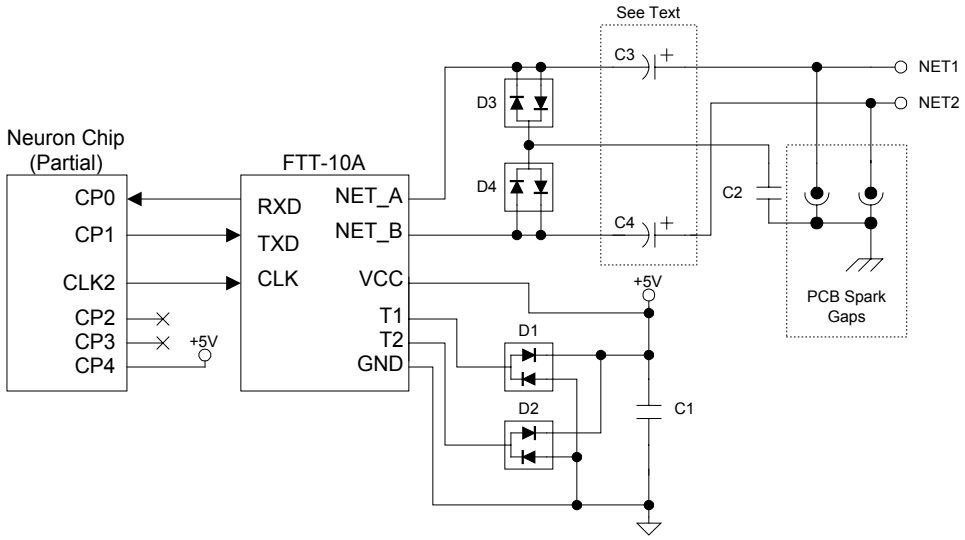


Figure 2.1 FTT-10A Transceiver Interconnection Using PCB Spark Gaps

Table 2.3 FTT-10A Transceiver External Components

Name	***Value***	***Comments***
C1	0.1µF for +5VDC decoupling	Power supply decoupling capacitor for FTT-10A transceiver
C2	1000pF, 2kV	ESD snubber capacitor
C3,C4	22µF, +50V, polar	DC blocking capacitors; see text
D1, D2, D3, D4	BAV99 or 1N4148(x2)	Transient clamping diodes; BAV99LT1 (National), BAV99LT (Sprague), MMBD120 (Motorola), or equivalent

Some applications cannot use PCB spark gaps due to the need for conformally coated or potted PCBs. In figure 2.2 the spark gaps are replaced with encapsulated discharge devices Z1 and Z2, which are connected to chassis ground. Each of these devices has a discharge voltage of approximately 300 volts and introduces very little capacitance (<1pF) to ground. Also note that diodes D3 through D6 are fast 1A rectifiers which survive level 3 surge voltages (see chapter 5) and load the network differentially with less than 150pF. These rectifiers are required to protect the FTT-10A transceiver from surge voltages seen differentially across Net1 and Net2 as a result of asymmetric firing of the discharge devices in the presence of surge voltages

coupled onto the network wiring. The physical placement of Z1 and Z2 should be near the entry points of the network wiring with a low impedance path to chassis ground (or alternately to star ground near star ground center). The external components for figure 2.2 are shown in table 2.4.

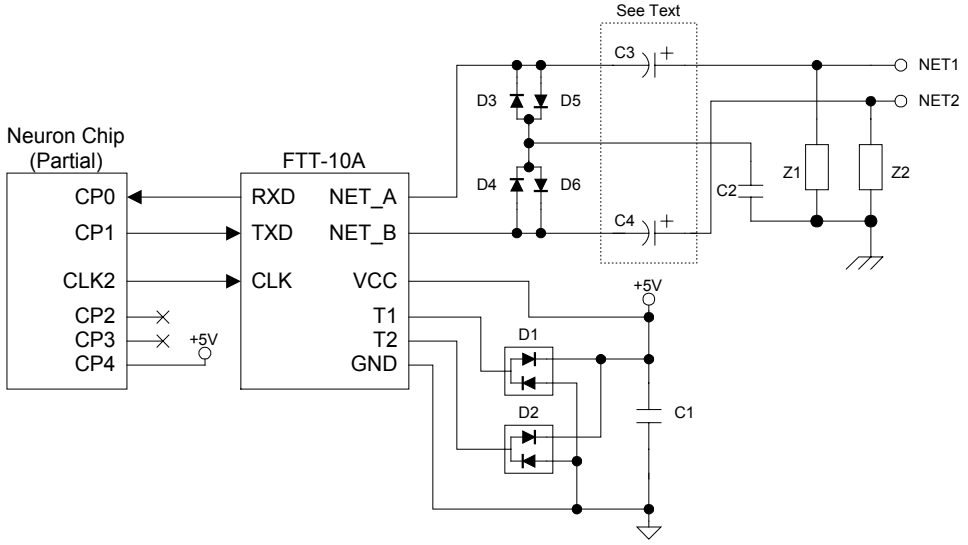


Figure 2.2 FTT-10A Transceiver Interconnection Using Discrete Spark Gaps

Table 2.4 FTT-10A Transceiver External Components

Name	***Value***	***Comments***
C1	0.1µF for +5VDC decoupling	Power supply decoupling capacitor for FTT-10A transceiver
C2	1000pF, 2kV	ESD snubber capacitor
C3,C4	22µF, +50V, polar	DC blocking capacitors; see text
D1, D2	BAV99 or 1N4148(x2)	Transient clamping diodes; BAV99LT1 (National or Motorola), BAV99LT (Sprague), or equivalent
D3, D4, D5, D6	1N4934, 1N4935	Fast switching rectifiers (General Instruments); Vishay-Liteon SMT diodes FR1D, RS1D, RS1DB
Z1, Z2	DSP-301N	Fast surge protectors with microgap (source: Mitsubishi Materials Corporation at US phone number +1-847-577-0200, or fax number +1-847-577-0201 or Europe (London) phone +44-171-236-0130)

Some applications require compliance only with Level 4 of the preferred contact-discharge method for electrostatic discharge (ESD) as defined in EN 61000-4. For these applications, diodes D3 and D4, and capacitor C2, as shown in figure 2.1, can be deleted. This simplified circuit has been tested at Level 4 under the preferred contact-discharge method for electrostatic discharge (ESD) in accordance with EN

61000-4. Note that it is the operation of the Neuron Chip, and not of the FTT-10A transceiver, which is affected at higher air-discharge levels when using the modified circuit. **It is recommended that the simplified circuit be used only after determining that contact-discharge ESD protection is acceptable for the application. If air-discharge ESD protection is required or the need for it is undefined or unknown, then the circuit shown in figure 2.1 or 2.2 should be used.**

The clock, reset, and power supply bypass circuits in the modified circuit will not represent a complete schematic, since they will vary depending on the Neuron Chip type and application. For complete Neuron Chip application schematics and information, refer to the *Neuron Chip Databook*[2,3]. See Chapter 3 for mechanical specifications and printed circuit board (PCB) footprint information. **See Chapter 5 (1000-4-6 testing) to determine if a network isolation common-mode choke is required for EMC compliance.**

In all of the interconnection schematics, capacitors C3 and C4 are used to provide DC voltage isolation for the FTT-10A transformer when the transceiver is used on a link power network, and may also be used to protect the transformer in the event of a DC fault on the network. The capacitors are required to meet LonMark interoperability guidelines. The capacitors are not needed on nodes that will be connected exclusively to non-link power networks and do not require protection against DC faults. Two polar capacitors are used to protect against the application of DC of either polarity while providing total net capacitance of 11µF. Alternatively, a single non-polar capacitor of 10µF may be used in either of the two legs which connect to the network. The initial tolerance of the capacitor should be ±20% or less, and degradation due to aging and temperature effects should not exceed 20% of the initial minimum value.

Network Connection

The network connection (NET1 and NET2) is polarity insensitive and therefore either of the two twisted pair wires can be connected to either of these network connections. Details about network wiring are discussed in chapter 5.

Clock Input

The FTT-10A transceiver receives its clock input from the Neuron Chip via the CMOS input CLK pin. This pin is driven by the CLK2 output of the Neuron Chip, whether the Neuron Chip's oscillator or an external clock oscillator is used. The CLK2 trace length should be kept to no more than 2cm (0.8”) to minimize noise coupling.

The FTT-10A transceiver operates with an input clock of 5, 10 or 20MHz. The transceiver automatically detects the clock rate and configures internal circuitry appropriately.

The accuracy of the input clock frequency to the Neuron Chip and transceiver must be ±200 ppm or better; this requirement can be met with a suitable crystal, but cannot be met with a ceramic resonator.

Neuron Chip Communications Port (CP) Lines

The FTT-10A transceiver transmits and receives LonTalk network packets via the Neuron Chip's direct, single-ended mode interface using pins CP0 and CP1. Neuron Chip data input pin CP0 is connected to the RXD pin of the FTT-10A transceiver. Neuron Chip data output pin CP1 is connected to the TXD pin of the FTT-10A transceiver. No buffering or other connections should be made to CP1.

The other Neuron Chip CP pins (CP2, 3, 4) are not connected to the FTT-10A transceiver. The transceiver automatically detects activity on its TXD pin to enable transmission, thus there is no connection to the Neuron Chip TXEN function on CP2. The FTT-10A transceiver has a built-in bias circuit to prevent transmission during the Neuron Chip reset process, when CP1 is not driven. The unused CP4 input should be connected to Vcc to prevent excess supply current draw in the Neuron Chip input buffer. Table 2.5 summarizes connections between the Neuron Chip Communication Port and the transceiver.

Table 2.5 Neuron Chip Communication Port Connections

Neuron Chip Pin	*Neuron Chip Function*	*Connect to*
CP0	Data input	FTT-10A RXD
CP1	Data output	FTT-10A TXD
CP2	Transmit enable output	Not connected
CP3	~Sleep output	Not connected
CP4	~Collision Detect input	Vcc

PC Board Layout Guidelines

An example of a PC board layout is shown in figure 2.3. The layout uses surface mount (SMT) components on the top side of the PCB. The scale of the figures is approximately 4X, but they are not intended for use as finished PCB artwork. Variations on this suggested PCB layout are possible as long as the general principles discussed later in this section (and in chapter 5) are followed. Through-hole capacitors and diodes can be used, but SMT components will generally be superior because of their lower series inductance.

Electrostatic discharge (ESD) and electromagnetic interference (EMI) are two of the most important design considerations when laying out the PCB for a node. These topics are discussed in general terms in chapter 5, and the specifics relating to PCB layout issues are covered here.

Tolerance of ESD and other types of network transients requires good layout of the power, ground and other node circuitry. In general, an ESD discharge current will return to earth ground or other nearby metal structures. The node's ground scheme must be able to pass this ESD current between the network connection and the node's external ground connection without generating significant voltage gradients

across the node's PCB. The low-inductance "Star" ground scheme illustrated in figure 2.4 and discussed below accomplishes this task.

1. **"Star" Ground Configuration:** The distribution of functional circuit blocks on the PCB should be in the form of a star, with the power connector, network connector and any "chassis ground" connection all located as close as practical to the center of the star. This star ground distribution is illustrated in figure 2.4. The goal of star ground distribution is to conduct transients out of the node with minimal disruption to other function blocks. If the node has a metal chassis, then ESD and other transients will generally return to that chassis via the star ground center point. If the node's logic ground is connected to this chassis ground, then connection should be made at this single point only. (Note that logic ground and chassis ground are shown connected in figures 2.3 and 2.4.) If a node is housed in a plastic enclosure and is powered with an isolating transformer, then there may not be any explicit earth ground or "chassis" ground available. In this case, it is still important for the network connector and power supply connector to be located near the center of the star.

2. **PC Board Spark Gaps and ESD Keepout Area:** The PC board layout should be designed so that substantial ESD hits from the network will discharge directly to the star ground center point. This is accomplished by creating PCB spark gaps from NET1 and NET2 to ground as detailed in figure 2.4. This design yields a metal-to-metal spacing on the PC board of 0.39mm (0.015”), which permits ESD hits above roughly 3kV to discharge directly to ground. This limits the amount of energy that must be absorbed by the FTT-10A transceiver and its associated circuitry. The keep-out area noted in figure 2.3 is designed to eliminate unintended discharge paths. If the PC board must be conformally coated or otherwise insulated, please refer to figure 2.2 for an alternate schematic that does not rely on exposed metal spark gaps.

3. **D1/D2 Clamp Diodes:** The diodes D1 and D2 clamp the node side of the FTT-10A transformer signals between Vcc and ground. The Vcc and ground connections between D1, D2, and the FTT-10A transceiver must be made using the low inductance technique shown in figure 2.3 to ensure that transient energy remaining after any discharge to the spark gaps does not disrupt the FTT-10A transceiver or the Neuron Chip. Note that the Vcc and ground connections of diodes D1 and D2 are designed to return transient currents to the FTT-10A ground pin and the star ground center point.

4. **D3/D4 Clamp Diodes:** The diodes D3 and D4 in figure 2.1 (D3 through D6 in figure 2.2) clamp the network side of the FTT-10A transformer signals to ground through C2 during ESD transients. The connections between D3, D4, and C2 must be made using the low inductance technique shown in figure 2.3 to ensure that transient energy remaining after any discharge to the spark gap does not disrupt the Neuron Chip. Note that the connection of C2 is designed to return transient currents to the star ground center point.

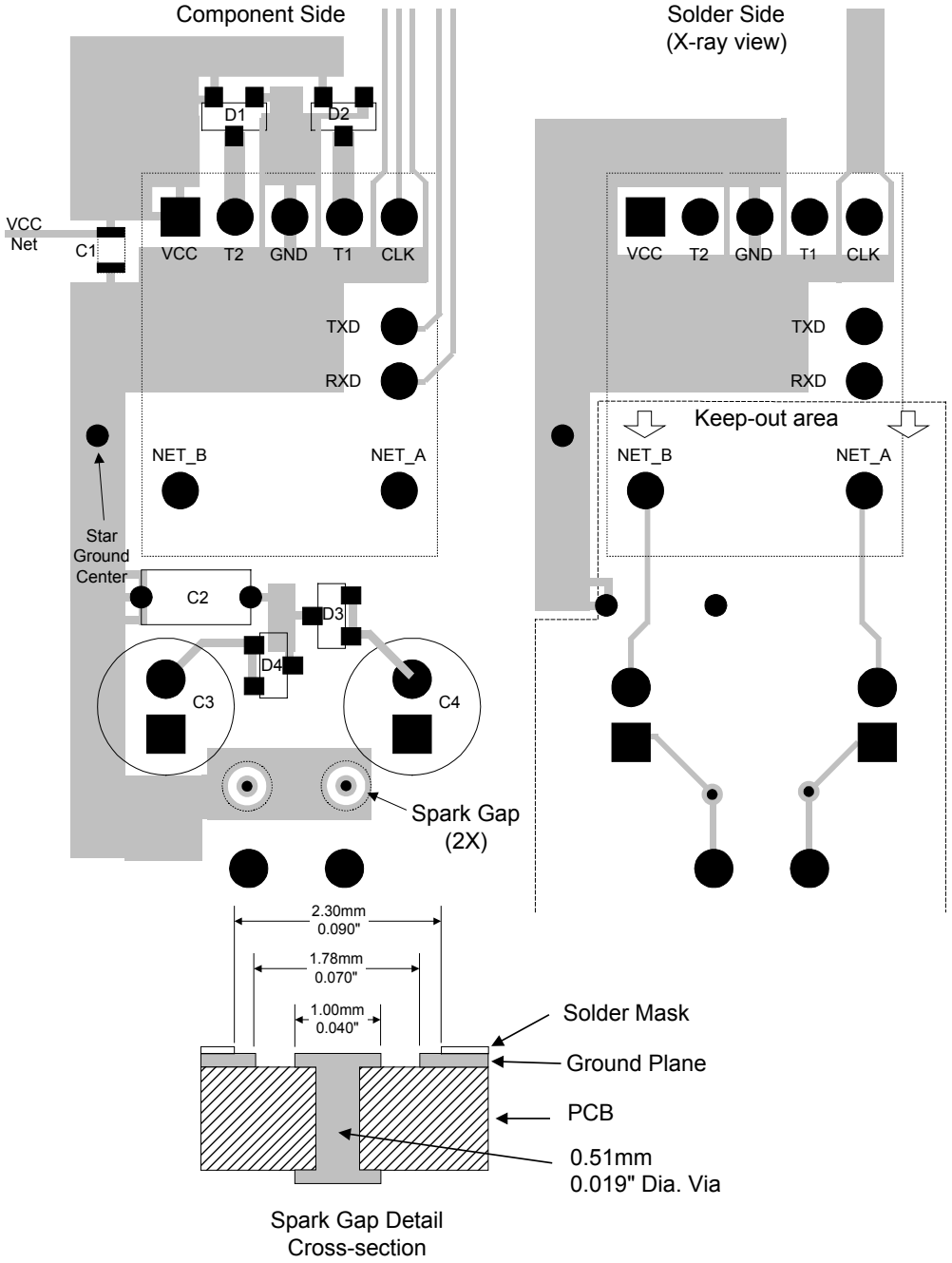


Figure 2.3 FTT-10A PCB Layout

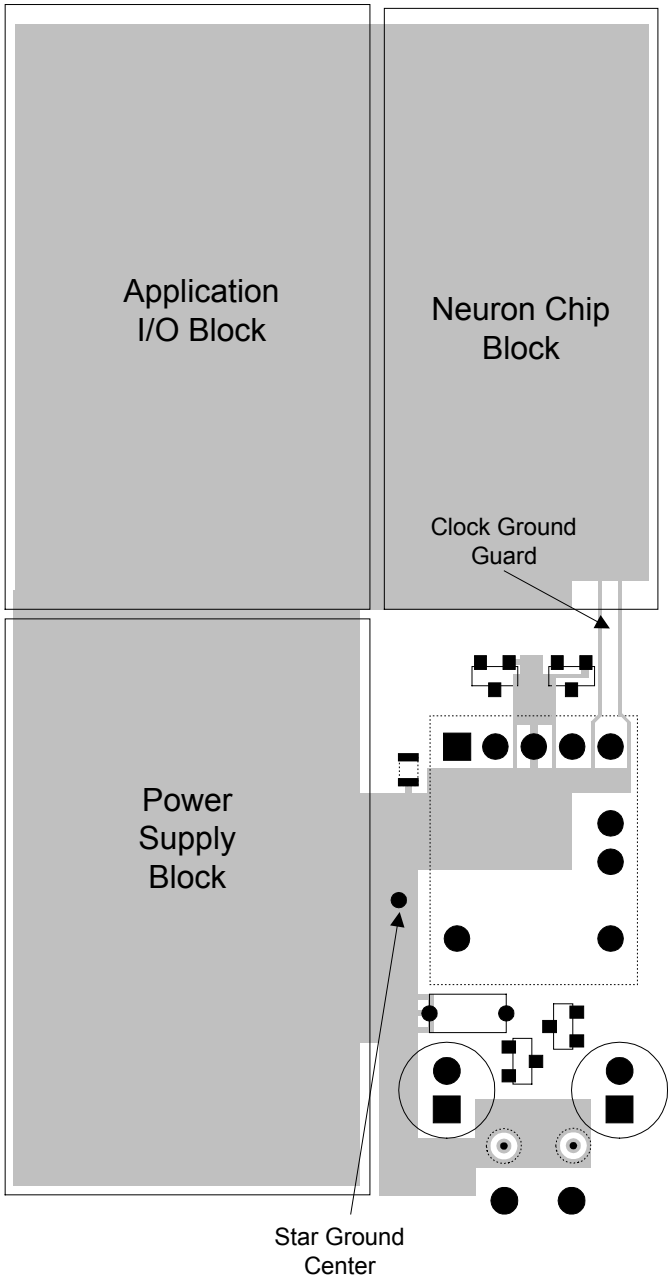


Figure 2.4 Star Ground Design

(Ground Distribution is Shown for Clarity Only)

5. **Ground Planes:** As ground is routed from the center of the star out to the function blocks on the board, planes or very wide traces should be used to lower the inductance (and therefore the impedance) of the ground distribution system.

6. **+5V Power Distribution & Decoupling:** In general, Vcc should be distributed through low inductance traces and planes in the same manner as ground. At least two 0.1µF SMT decoupling caps are recommended around the Neuron Chip on the component side of the PCB; follow the recommendations in the Neuron Chip Databooks[2,3]. In contrast to the wide Vcc distribution to the Neuron Chip and other node circuitry, the routing of Vcc to the FTT-10A transceiver should be through a narrow trace of 0.3mm (0.012 inch) width. The inductance of this trace in combination with the FTT-10A transceiver's Vcc decoupling capacitor, C1, helps to reduce digital noise at the FTT-10A transceiver's Vcc input (pin 1), which reduces EMI on the network wiring. Place C1 immediately next to the FTT-10A transceiver as shown in figure 2.3.

7. **CLK Routing for EMI Control:** The CLK input to the FTT-10A needs to be guarded by ground traces to minimize clock noise, and to help keep EMI levels low (see chapter 5). In general, the Neuron Chip should be placed close enough to the FTT-10A transceiver and oriented correctly so that the CLK trace from the Neuron Chip to the transceiver is no longer than 2cm (0.8"). At the same time, the Neuron Chip and any other fast digital circuitry should be kept away from the network connector and NET_A/NET_B pins (pins 2 and 3) on the transceiver. If noisy digital circuitry is located too close to the network connector, RF noise may couple out onto the network cable and cause EMI problems.

8. **FTT-10A Transceiver Grounding for EMI Control:** To best control EMI, the connection between the FTT-10A transceiver ground pin and the center of star ground should be wide and short as shown in figure 2.3.

9. **Avoiding Magnetic Field Interference With The FTT-10A Transceiver**: As with all tranformer-coupled data communication transceivers, it is important to keep sources of stray magnetic field noise from interfering with network communication. A complete discussion on avoiding and managing magnetic field interference can be found in Appendix D.

Physical Layer Repeater

In the event that the limits on the number of transceivers or total wire distance are exceeded, a physical layer repeater (figure 2.5) can be added to interconnect two or more TP/FT-10 network segments. This effectively multiplies overall channel capability, including node count and network extent, but not bandwidth. Note that only one physical layer repeater shoud be placed in series between any two nodes on a channel. If additional cabling or network bandwidth are required, then a LONWORKS Router such as Echelon's LPR-10 Model 42100 should be used in place of a repeater.

Designing large networks which rely on physical layer repeaters to extend node count requires careful consideration of network traffic. Testing of the network under worst-case traffic conditions while monitoring with a LonManager Protocol Analyzer is highly recommended to properly evaluate system performance. LONWORKS Routers and/or topology changes may be used to solve traffic congestion problems.

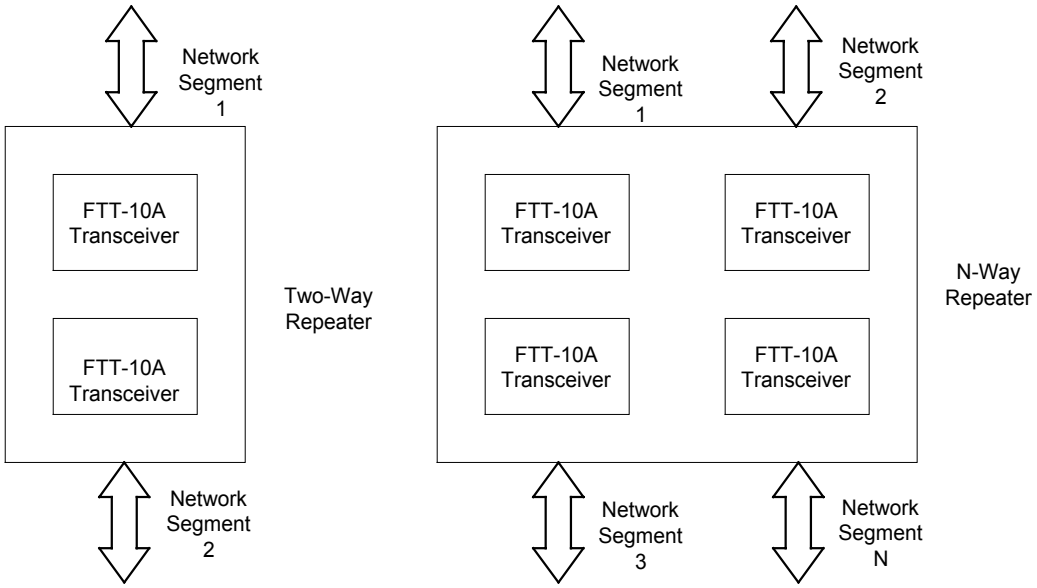
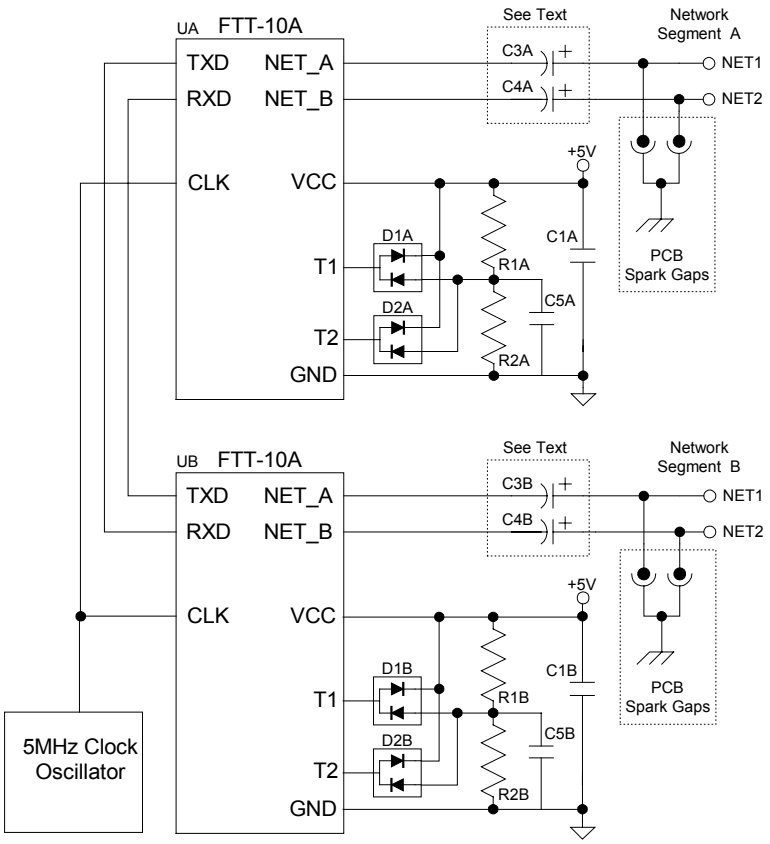


Figure 2.5 Two-Way and N-Way Repeaters

A repeater consists of two or more transceivers, a 5MHz clock source, and miscellaneous components. Figures 2.6 and 2.7 show schematics for two-way and N-way repeaters, respectively, for use where the operating temperature range does not exceed 0 to +85°C. Figure 2.8 shows a more complex design for operating temperatures from -40 to +85°C, which uses a PAL that requires programming with one of the JEDEC files shown in Appendix C. The clock oscillator requires CMOS output levels, ±200 ppm total accuracy (use only a crystal-controlled oscillator; do not use a ceramic resonator-controlled oscillator), and duty cycle between 40/60 and 60/40. The OR gate in figure 2.7 requires CMOS output levels and 100nsec maximum propagation delay. No ESD snubber diodes or capacitors are shown in figures 2.6 through 2.8 because the FTT-10A transceivers (without accompanying Neuron Chips) do not require them. Resistors R1, R2 and capacitor C5 shown in figures 2.6 and 2.7 are required for proper repeater operation.

Refer to information earlier in this chapter on PC board layout guidelines. **To prevent magnetic coupling between transceivers, maintain a minimum edge-to-edge spacing of 2.5cm (1 inch) between adjacent transceivers.**



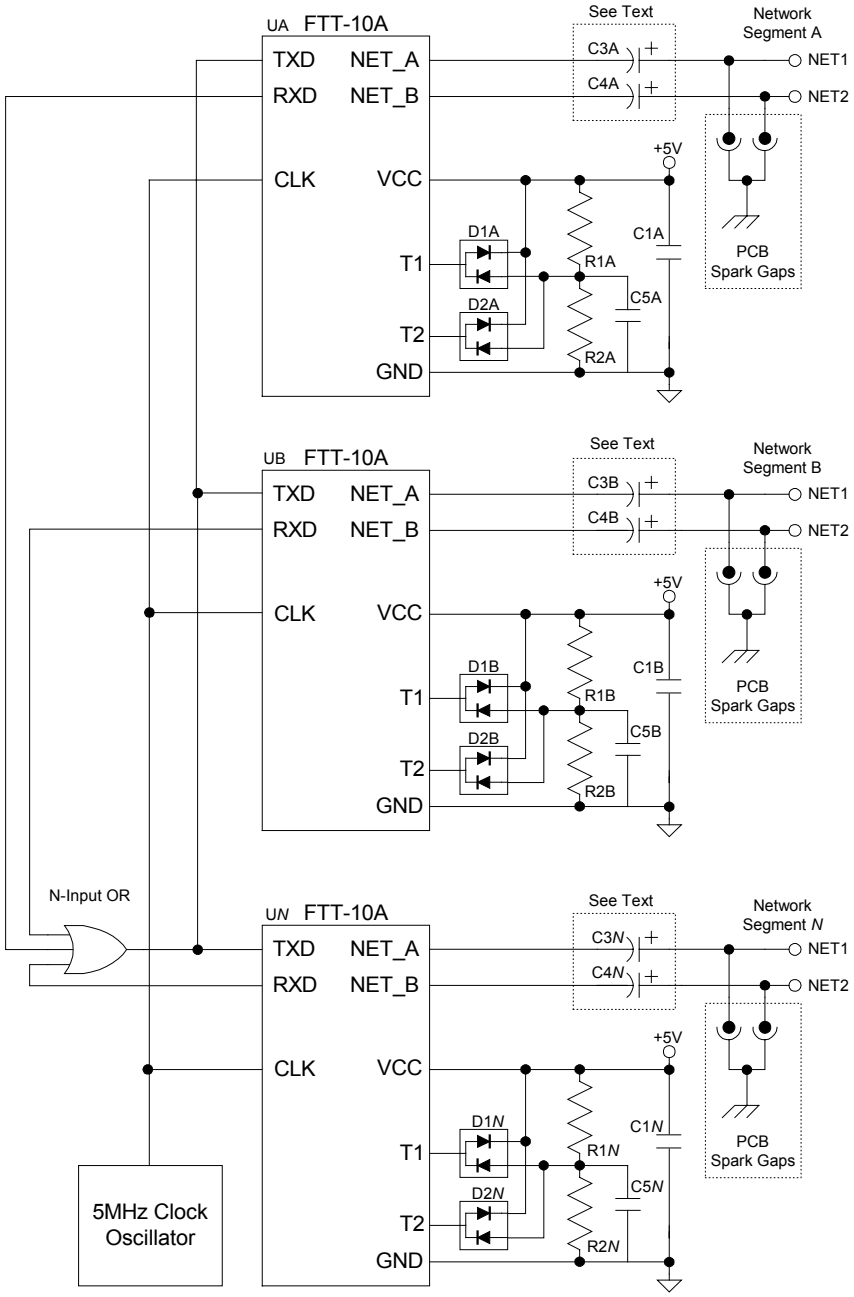
R1 1500Ω, 1%, 1/10W

R2 576 Ω, 1%, 1/10W

C5 0.1 µF, X7R or Y5V ceramic

Other components per table 2.3

Figure 2.6 Two-Way Repeater Schematic (0 to +85C)



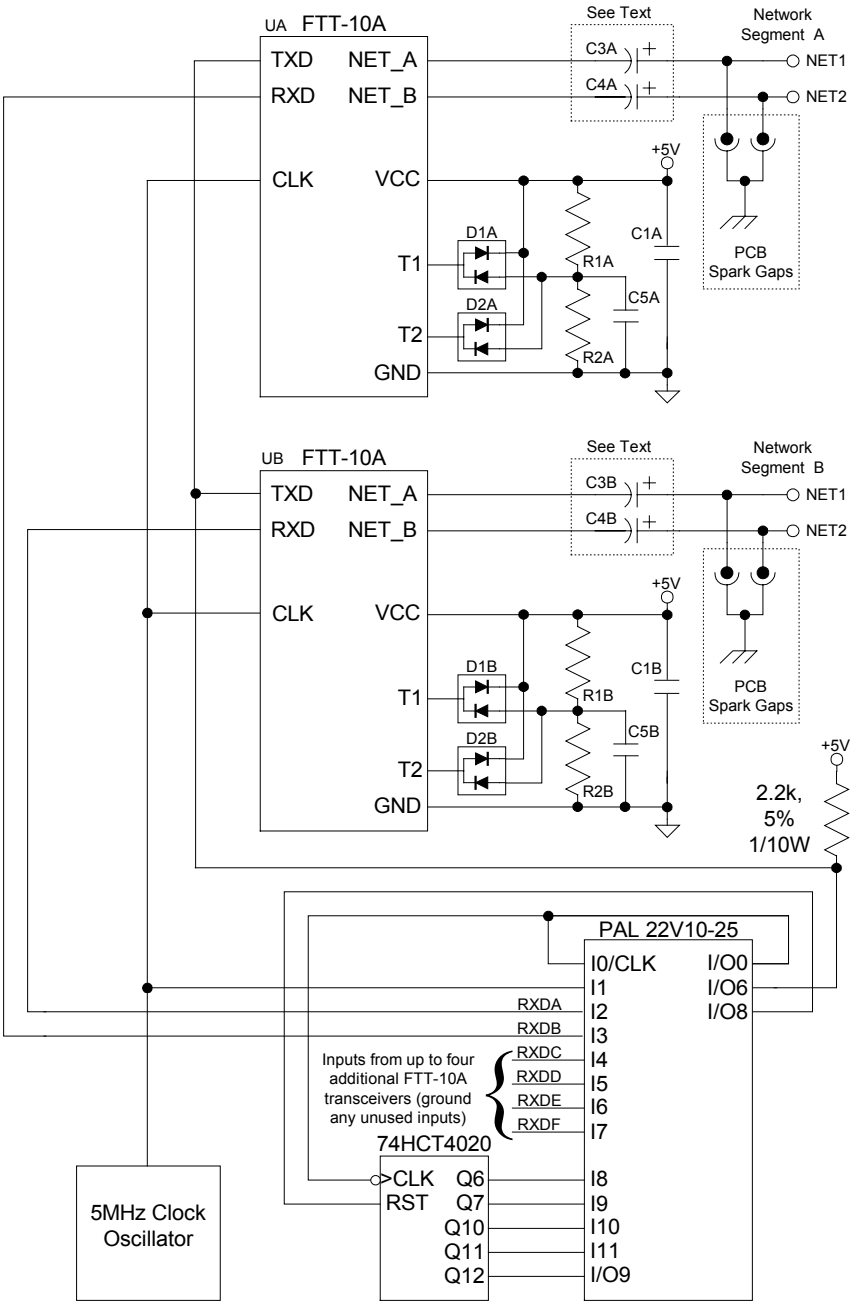
R1 1500Ω, 1%, 1/10W

R2 576 Ω, 1%, 1/10W

C5 0.1 µF, X7R or Y5V ceramic

Other components per table 2.3

Figure 2.7 N-Way Repeater Schematic (0 to +85C)



R1 1500Ω, 1%, 1/10W

R2 576 Ω, 1%, 1/10W

C5 0.1 µF, X7R or Y5V ceramic

Add power supply bypass capacitors (not shown) next to oscillator, 74HCT4020 and PAL

PAL requires programming: see text

Other components per table 2.3

Figure 2.8 2-Way to 6-Way Repeater Schematic (-40 to +85°C)

3

Mechanical Considerations

This chapter discusses the mechanical footprint and pin locations of the FTT-10A Free Topology Transceiver.

Mechanical Footprint

The FTT-10A transceiver mechanical dimensions are shown in figures 3.1 through 3.4. The transceiver is mounted to the application board as a through-hole, soldered component. Decisions about component placement on the application electronics board must also consider electromagnetic interference (EMI) and electrostatic discharge (ESD) issues as discussed elsewhere in this document.

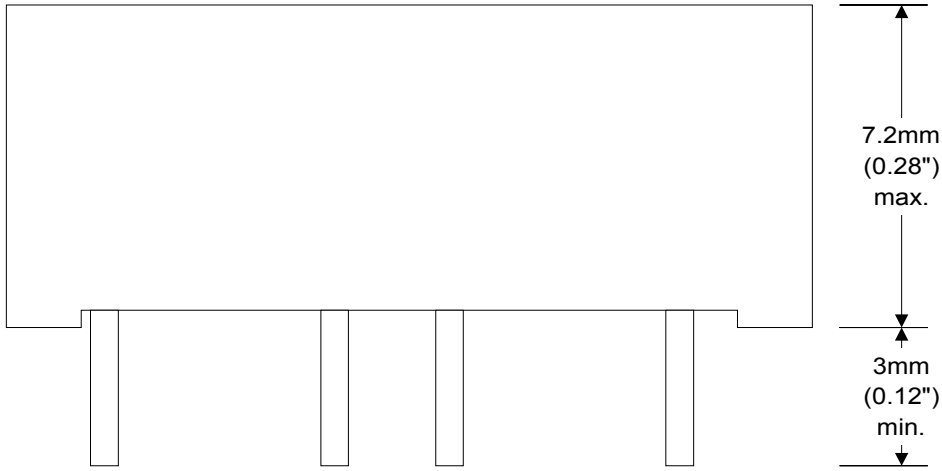


Figure 3.1 FTT-10A Transceiver Side View

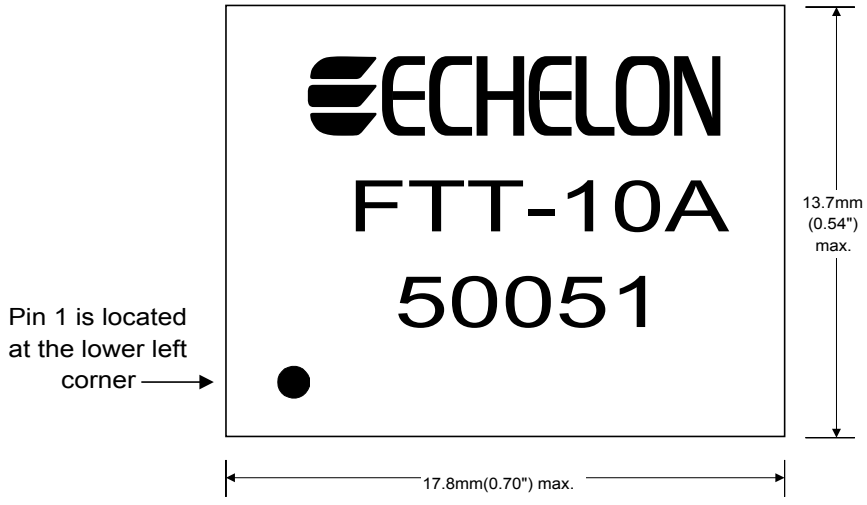
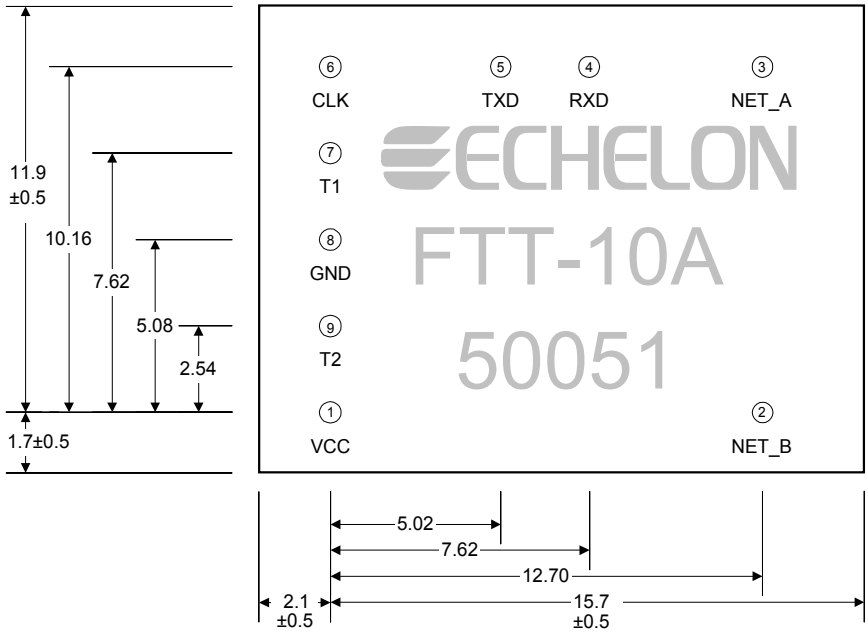


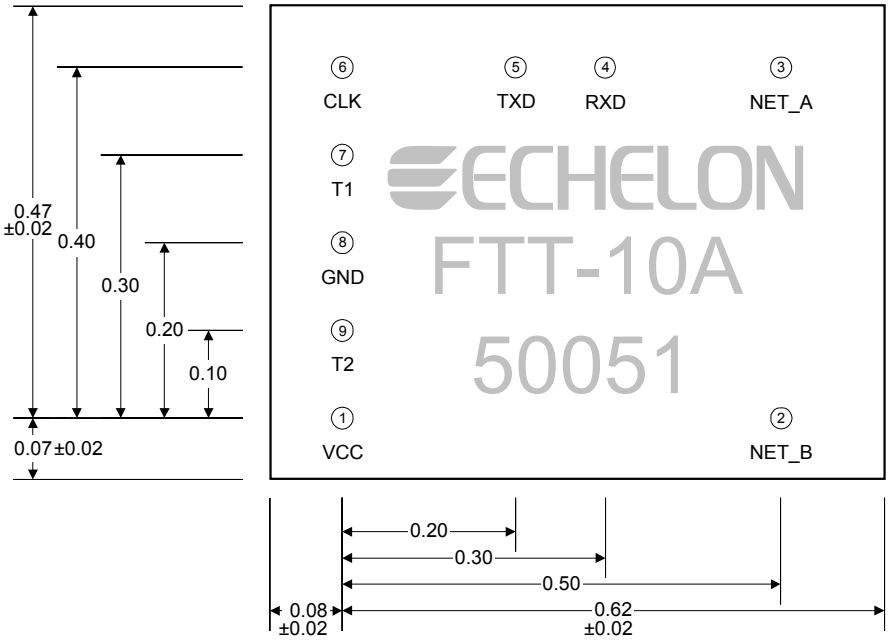
Figure 3.2 FTT-10A Transceiver Top View



Pin diameter is 0.60+0.10/-0.15 mm

Pin locations are ±0.25mm from ideal 2.54mm grid

Figure 3.3 FTT-10A Transceiver Top "X-RAY" View – dimensions in mm



Pin diameter is 0.024+0.003/-0.007 inches

Pin locations are ±0.01 inches from ideal 0.10 inch grid

Figure 3.4 FTT-10A Transceiver Top "X-RAY" View – dimensions in inches

4

Network Cabling and Connection

This chapter provides information about cabling and network connections for the FTT-10A Free Topology Transceiver.

Network Topology Overview

The TP/FT-10 network is designed to support free topology wiring, and will accommodate bus, star, loop, or any combination of these topologies. FTT-10A transceivers can be located at any point along the network wiring. This capability simplifies system installation and makes it easy to add nodes should the network need to be expanded. Figures 4.1 through 4.5 present five different network topologies. Note that the actual termination circuit will vary by application.

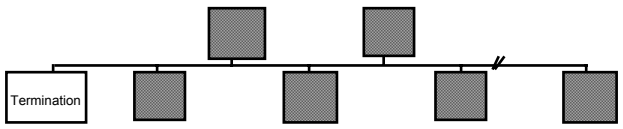


Figure 4.1 Singly Terminated Bus Topology

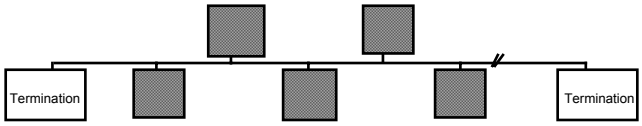


Figure 4.2 Doubly Terminated Bus Topology

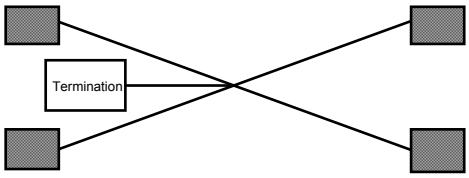


Figure 4.3 Star Topology

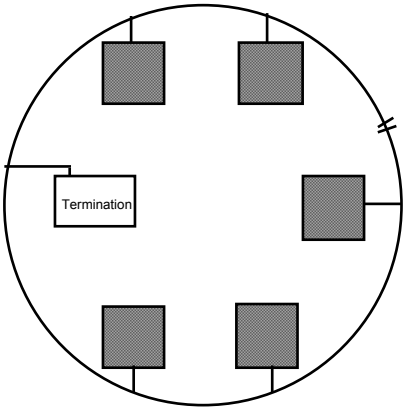


Figure 4.4 Loop Topology

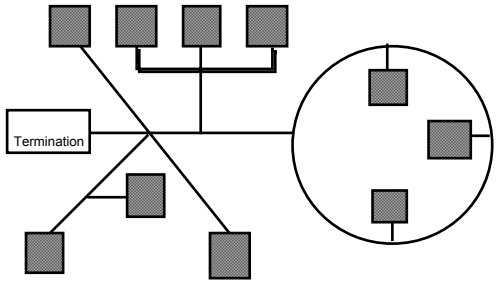


Figure 4.5 Mixed Topology

In the event that the limits on the number of transceivers or total wire distance are exceeded, then one FTT physical layer repeater can be added to interconnect two segments and double the overall system capability (see chapter 2). The FTT-10A transceiver can also be used with LONWORKS Routers, such as the LPR-10 Model 42100, to interconnect a TP/FT-10 channel with another TP/FT-10 channel, or with any other LONWORKS channel.

System Performance and Cable Selection

TP/FT-10 networks must meet the System Specifications and Transmission Specifications as outlined below. When creating documentation and installation procedures for TP/XF-10 networks, be sure to include the TP/FT-10 System Specifications and, based upon the cable used, the appropriate Transmission Specification listed below. Incorporating these specifications will ensure a smoother installation and provide a resource for the installer who must troubleshoot the installation.

Echelon has qualified a variety of cables for use with TP/FT-10 networks. Based on the cost, performance, and availability of these different cable types, system designers can choose the most appropriate cable for their application. Echelon has qualified three "generic" cable types, as follows:

- A generic 16AWG (1.3mm diameter) cable (similar to Belden 85102);
- NEMA Level 4 cable (this cable is ***not*** equivalent to TIA Category IV cable); and
- TIA Category 5 cable.

The electrical specifications for these cables can be found in Appendix E. A list of cable vendor can be found in the *Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks* engineering bulletin (005-0023-01). This bulletin can be found on Echelon's web site at www.echelon.com in the documentation menu of the Products section. These cables have been qualified by Echelon in a generic form, and are available from vendors in a number of variations, including shielded, unshielded, plenum, and non-plenum jacketing. Additionally, Echelon has qualified two 16AWG (1.3mm) Belden cables, and one cable used in specific applications in the European market (JY(St)Y).

Note that the following specifications are for one network segment. Multiple segments may be combined using repeaters as described in chapters 1 and 2 to increase the number of nodes and distance.

System Specifications

- Up to 64 FTT-10A transceivers are allowed per network segment.
- LPT-10 transceivers may be used on network segments with FTT-10A transceivers, but are subject to additional constraints, particularly on distance. See the *LONWORKS LPT-10 Link Power Transceiver User's Guide* for more information.
- The average temperature of the wire must not exceed +55°C, although individual segments of wire may be as hot as +85°C.
- As a general rule, the TP/FT-10 channel communication cables should be separated from high voltage power cables. Follow local electrical codes with regard to cable placement.

Table 4.1 Doubly-Terminated Bus Topology Specifications

	Maximum bus length	***Units***
Belden 85102	2700	Meters
Belden 8471	2700	
Level IV, 22AWG	1400	
JY(St) Y 2x2x0.8	900	
TIA Category 5	900	

A doubly-terminated bus may have stubs of up to 3 meters from the bus to each node.

Table 4.2 Free Topology Specifications

	Maximum node-to-node distance	***Maximum total Wire length***	***Units***
Belden 85102	500	500	Meters
Belden 8471	400	500	
Level IV, 22AWG	400	500	
JY(St) Y 2x2x0.8	320	500	
TIA Category 5	250	450	

The free topology transmission specification includes two components that must both be met for proper system operation. The distance from each transceiver to all other transceivers and to the termination (including the LPI-10 termination, if used) must not exceed the *maximum node-to-node distance*. If multiple paths exist, e.g., a loop topology, then the longest path should be used for calculations. The *maximum total wire length* is the total length of wire within a segment.

Cable Termination and Shield Grounding: Terminators, Termination Procedures, and Grounding Circuits

TP/FT-10 network segments require termination for proper data transmission performance. The type of terminator varies depending on whether shielded or unshielded cable is used. Free topology and Bus networks also differ in their termination requirements. The following sections describe the various terminators and termination procedures.

Free Topology Network Segment

In a free topology segment, only one termination is required and may be placed anywhere on the free topology segment. There are two choices for the termination:

1. RC network (figure 4.6), with Ra = 52.3Ω±1%, 1/8W
2. LPI-10 Link Power Interface, with jumper at "1 CPLR" setting.

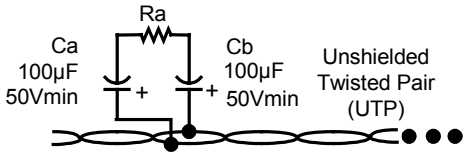
Doubly Terminated Bus Topology Segment

In a doubly terminated bus topology, two terminations are required, one at each end of the bus. There are two choices for each termination:

1. RC network (figure 4.6), with Ra = 105Ω±1%, 1/8W

2. LPI-10 Link Power Interface, with jumper at "2 CPLR" setting.

At this time, only **one** LPI-10 interface is supported per segment. The LPI-10 contains the two required terminators. The other terminator must be an RC-type (see figure below).



Notes:
1. Ca and Cb are typically aluminum-electrolytic type for improved longevity in the presence of ESD – observe polarity.
2. Ca and Cb are required for connection to link power networks and to meet LONMARK interoperability guidelines.

Figure 4.6 Twisted Pair Termination Network

Grounding Shielded Twisted Pair Cable

When using Shielded Twisted Pair, terminate the twisted pair **and** ground the cable shield, as shown in figure 4.7.

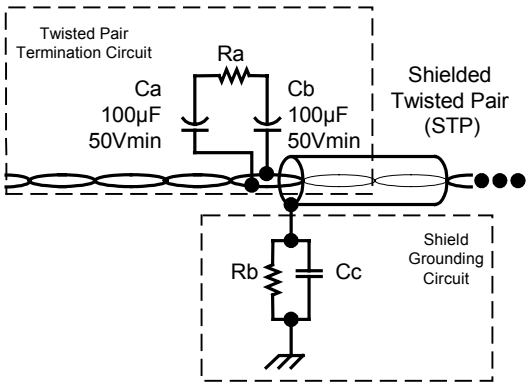


Figure 4.7 Terminating and Grounding Shielded Twisted Pair Cable

The twisted pair is terminated according to the guidelines listed in the previous sections. The cable shield should be grounded using a capacitor to tie the shield to earth ground, and a large-value resistor to bleed off any static charge on the shield.
Tie the shield to earth ground through a capacitor, instead of a direct connection, in order to avoid DC and 50/60 Hz ground paths from being formed through the shield. Typical values for Rb and Cc are as follows:

Cc = 0.1 μF, 10%, Metalized Polyester, ≥ 100V
Rb = 470kΩ, 1/4W, ±5%

The cable shield should be grounded at least once per segment, and preferably at each node. Grounding the shield at every node (using the shield grounding circuit shown in figure 4.7) will assist in suppressing 50/60Hz standing waves.

5

Design Issues

This chapter looks at design issues, and includes discussions of electromagnetic interference (EMI), electrostatic discharge (ESD), building entrance (lightning) protection, vibration, shock, and EN 61000-4 testing for the FTT-10A Free Topology Transceiver.

EMI Design Issues

The high-speed digital signals associated with microcontroller designs can generate unintentional electromagnetic interference (EMI). High-speed voltage transitions generate RF currents that can cause radiation from a product if a length of wire or piece of metal can serve as an antenna.

Products that use an FTT-10A transceiver together with a Neuron Chip will generally need to demonstrate compliance with EMI limits enforced by various regulatory agencies. In the USA, the FCC[6] requires that unintentional radiators comply with Part 15 level "A" for industrial products, and level "B" for products that can be used in residential environments. Similar regulations are imposed in most countries throughout the world[8].

In addition to the following discussion, designers of FTT-10A nodes are strongly encouraged to read reference [11] for a good treatment of EMC. The EDN Designer's Guide to EMC[12] also contains very good design advice.

Designing Systems for EMC (Electromagnetic Compatibility)

Careful PCB layout is important to ensure that an FTT-10A node will achieve the desired level of EMC. A typical FTT-10A node will have several digital signals switching in the 1-10MHz range. These signals will generate voltage noise near the signal traces, and will also generate current noise in the signal traces and power supply traces. The goal of good node design is to keep this voltage and current noise from coupling out of the product's package.

It is very important to minimize the "leakage" capacitance from circuit traces in the node to any external pieces of metal near the node, because this capacitance provides a path for the digital noise to couple out of the product's package. Figure 5.1 shows the leakage capacitances to earth ground from a node's logic ground ($C_{leak,GND}$) and from a digital signal line in the node ($C_{leak,SIGNAL}$). If the FTT-10A node is housed inside a metal chassis, then that metal chassis will probably have the largest leakage capacitance to other nearby pieces of metal. If the node is housed inside a plastic package, then PCB ground guarding must be used to minimize $C_{leak,SIGNAL}$. Effective guarding of digital traces with logic ground reduces $C_{leak,SIGNAL}$ significantly, which in turn reduces the level of common-mode RF currents driven onto the network cable.

When a node is mounted near a piece of metal, especially metal that is earth grounded, any leakage capacitance from fast signal lines to that external metal will provide a path for RF currents to flow. When V_{gate} is pulled down to logic ground, the voltage of logic ground with respect to earth ground will increase slightly. When V_{gate} pulls up to Vcc, logic ground will be pushed down slightly with respect to earth ground. As $C_{leak,SIGNAL}$ increases, a larger current flows during V_{gate} transitions, and more common-mode RF current couples into the network twisted pair. This common-mode RF current can generate EMI in the 30-500MHz frequency band in excess of FCC/CISPR "B" levels even when $C_{leak,SIGNAL}$ from a clock line to earth ground is less than 1pF. Guarding of clock lines is essential for meeting Level "B" limits.

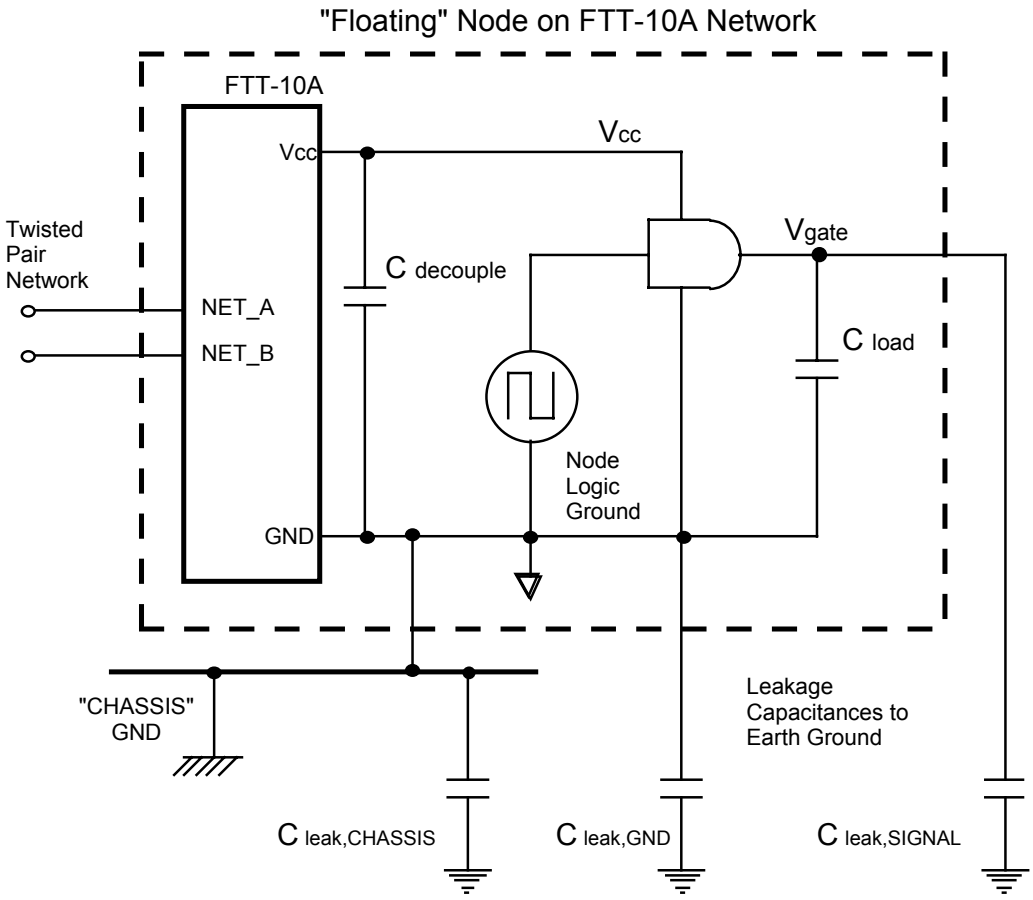


Figure 5.1 Parasitic Leakage Capacitances to Earth Ground

From this discussion, it is apparent that minimizing $C_{leak,SIGNAL}$ is very important. By using 0.1µF or 0.01µF decoupling capacitors at each digital IC power pin, Vcc and logic ground noise can be reduced. Logic ground can then be used as a ground shield for other noisy digital signals and clock lines.

For example, in most FTT-10A nodes that use the Neuron 3120 Chip, the fastest digital signal that needs to be routed across the PCB is the CLK2 line from the Neuron Chip to the FTT-10A transceiver. If a two-layer PCB is being used, CLK2 can be routed to the transceiver pin with ground guard traces straddling the clock trace on the top side of the board and a wide ground trace covering the underside of the clock trace on the bottom side. If a four-layer PCB is being used, the clock trace can be moved to an inner layer and guarded on all four sides. The CLK2 trace from the Neuron Chip to the FTT-10A transceiver should be as short as practical, and in all cases no more than 2cm.

Since the Neuron 3150 Chip has an external memory interface bus, there are many more traces that need to be guarded by logic ground in a Neuron 3150 Chip-based FTT-10A node. In addition, the Vcc noise generated by the memory interface and external ROM/RAM components requires more Vcc decoupling, and may require a four-layer PCB to maintain an RF-quiet Vcc and logic ground.

Some FTT-10A nodes with fast digital circuitry, such as DSP engines and memory arrays, may require extra RF attenuation between the FTT-10A transceiver and the twisted pair network in order to meet FCC/CISPR level "A" or "B". This extra attenuation can be provided by a ferrite bead (muRata BLM11A601 or equivalent) in series with each network line adjacent to the network connector. Each of these ferrite beads must have an inductance of no more than 30µH. Alternately, a common mode EMI choke (muRata PLT1R53C or equivalent) could be used in place of the two ferrite beads. If a common-mode choke is placed in series with the FTT-10A network connection, it must have less than 40pF of differential capacitance.

The network Isolation Choke (Appendix F) that is recommended for protection against large common-mode interference signals (like those encountered in EN 61000-4-6 testing, described at the end of this chapter) also provides significant attenuation of common mode network EMI currents up to 500MHz. Therefore, in many applications the Network Isolation Choke can be used in place of the EMI choke or ferrite beads. When substituting the Network Isolation Choke for the EMI choke or ferrite beads, the node should be re-tested for radiated EMI compliance.

Some amount of filtering may also be required on an FTT-10A node's power supply input, depending on the level of noise generated by the application circuitry. This is best accomplished by placing ferrite chokes in series with the power input traces adjacent to the power connector. A typical power supply circuit illustrating the placement of these ferrite chokes is shown in figure 5.2.

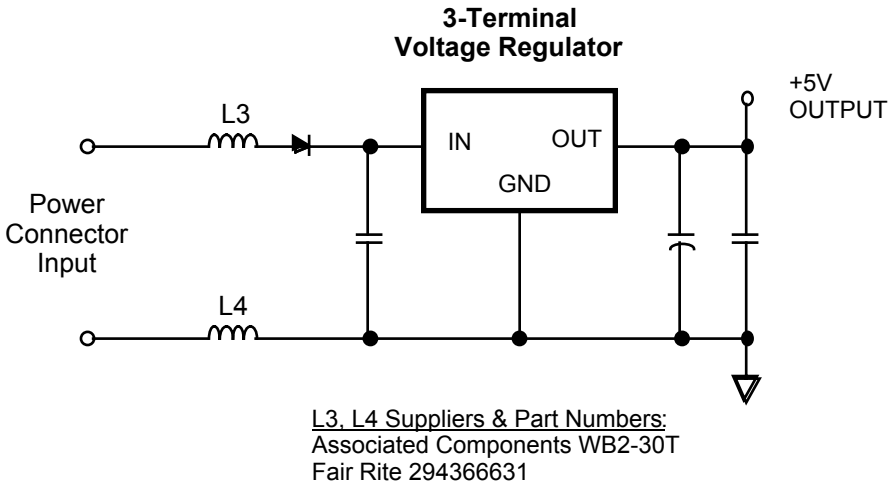


Figure 5.2 Illustration of Power Supply Input Filtering Using Ferrite Chokes

In summary, the following general rules apply:

- the faster the Neuron Chip clock speed, the higher the level of EMI;
- better Vcc decoupling quiets RF noise at the sources (the digital ICs), which lowers EMI;
- the Neuron 3120 Chip will generate less EMI than the Neuron 3150 Chip since the Neuron 3120 Chip has no external memory interface lines;
- a four-layer PCB will generate less EMI than a two-layer PCB since the extra layers facilitate better Vcc decoupling and more effective logic ground guarding;

- a two-layer FTT-10A node should be able to meet FCC/CISPR level "B" EMC if good decoupling and ground guarding are used;
- ferrite beads in series with the network traces at the network connector, and ferrite chokes in series with the power input traces at the power connector, can be used to help meet EMC requirements for nodes that have noisy application circuitry or special circuit requirements.

Early testing of prototype circuits at an outdoor EMI range should be used to determine the effectiveness of these EMC techniques in a particular application.

ESD Design Issues

Electrostatic discharge (ESD) is encountered frequently in industrial and commercial use of electronic systems[10]. In addition, the European Community has adopted requirements for ESD testing[13].

Reliable system designs must consider the effects of ESD and take steps to protect sensitive components. Static discharges occur frequently in low-humidity environments when operators touch electronic equipment. Keyboards, connectors, and enclosures may provide paths for static discharges to reach ESD sensitive components such as the Neuron Chip and the FTT-10A transceiver. This section describes the issues involved in designing ESD immunity into FTT-10A transceiver-based products.

In addition to the following discussion, designers of FTT-10A nodes are strongly encouraged to read references [10] and [12]. The *EDN Designer's Guide to EMC*[12] is especially helpful in understanding the importance of managing ESD return currents.

Designing Systems for ESD Immunity

There are two general methods that are used to "ESD harden" products. The first is to seal the product to prevent static discharges from reaching the sensitive circuits inside the package. The second method involves designing the grounding of a product so that ESD hits to user-accessible metal parts can be shunted around any sensitive circuitry.

Since the network connector is user-accessible, it is not possible to totally seal FTT-10A nodes. However, the product's package should be designed to minimize the possibility of ESD hits arcing into the node's circuit board. If the product's package is made of plastic, then the PCB should be supported in the package so that unprotected circuitry on the PCB is not adjacent to any seams in the package. The PCB should not touch the plastic of an enclosure near a seam, since a static discharge can "creep" along the surface of the plastic, through the seam, and arc onto the PCB.

Once an ESD hit has arced to the product, the current from the discharge will flow through all possible paths back to earth ground. The grounding of the PCB and the protection of user-accessible circuitry must allow these ESD return currents to flow back to earth ground without disrupting normal circuit operation of the Neuron Chip

or other node circuitry. Generally, this means that the ESD currents should be shunted to the center of a star ground configuration (see chapter 2) and then out to the product's chassis or earth ground connection. If the node is floating with respect to earth ground, the ESD current will return capacitively to earth via the network wire, the power supply wires, and the PCB ground plane.

Designers of FTT-10A transceiver-based nodes should follow the PCB layout guidelines presented in chapter 2. In addition, external clamping of user-accessible circuitry is required to shunt ESD currents from that circuitry to the center of the star ground on the PCB. For example, if the Neuron Chip in an FTT-10A node is scanning a keypad with some of its I/O lines, then the I/O lines to that keypad will need to be diode-clamped as shown in figure 5.3. If a negative ESD hit discharges into the keypad, then the diode clamps to ground shunt the ESD current into the ground plane. If a positive ESD hit discharges into the keypad, then the Vcc diodes shunt the current to the ground plane via a 0.1µF decoupling capacitor that is placed directly adjacent to the clamp diodes. The keypad connector, diodes and decoupling capacitor should all be located close to the center of the star ground so that the ESD current does not pass through sensitive circuitry on its way out of the PCB.

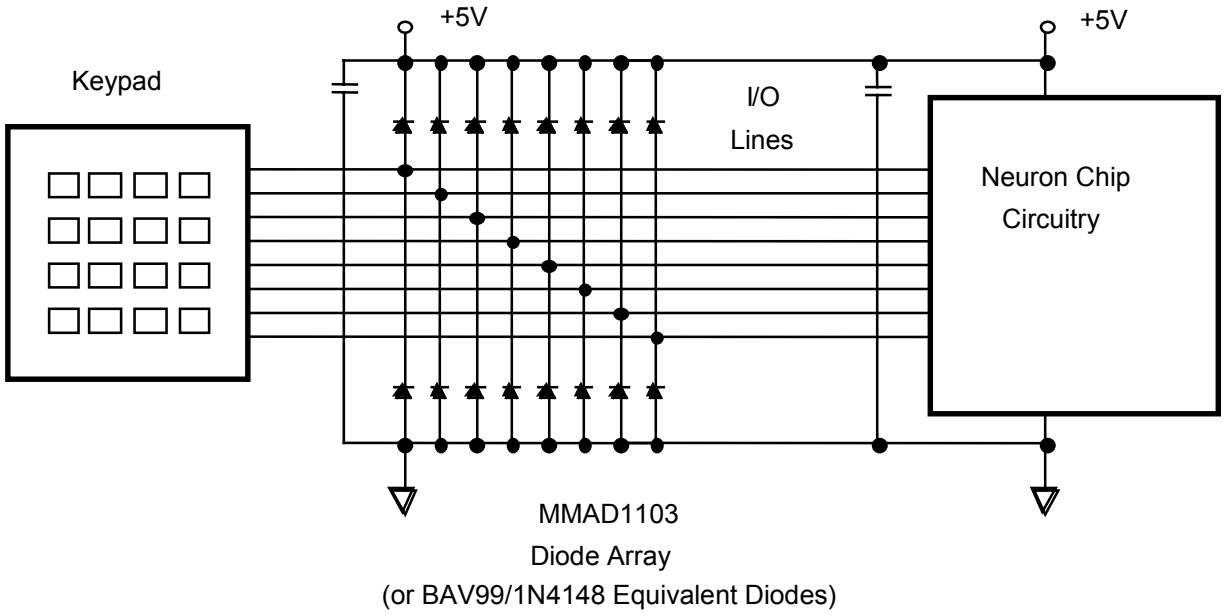


Figure 5.3 Illustration of I/O Line ESD Clamps

Building Entrance Protection

Echelon recommends using shielded twisted pair wire for all networks, or portions of networks, that are run outside of buildings. The shield should be connected to earth at each building entry point via a data lightning/surge arrester, to conduct excessive surges or lightning strike energy to ground and prevent their entry inside the building via the network. Data line lightning/surge arresters should also be used at each building entrance and connected to the network data lines. Therefore, two additional arresters, one for each conductor of the twisted pair, are required, and the arresters must be of the gas discharge type to minimize any corruption of the network data traffic. MOV and TVS protection devices must not be used on the network data lines since the intrinsically higher capacitance of these devices will corrupt, or even prevent, network traffic between nodes.

Gas discharge technology is typically used for data line lightning/surge arresters due to its very low capacitance (typically < 5pF) and rapid response. Low capacitance gas discharge arresters do not have any impact on the maximum number of nodes possible on a network segment. Note that for each 300 picofarads of protection circuitry capacitance connected to the network, the FTT-10A node count must be reduced by one. For example, if two lightning/surge arresters, each presenting a 300 picofarad load, are used in the network, then the maximum number of nodes allowed on that physical segment will be 64 minus 2, or 62 nodes. When using link power networks, the capacitance limit per link power node is 150 picofarads; if the lightning/surge arrester set presents 150 picofarads to the network cable at both entrances, the maximum number of link power nodes is reduced to 128 to 126 nodes. The above limits apply to any contiguous network segment. Repeaters and routers physically isolate their two segments so the limits stated apply to each segment. Also, due to the minimal amount of "leakage capacitance" to ground allowed in a link power network, the two arresters at each entrance in a link power network segment must be balanced to within 10 picofarads.

The following figure depicts twisted pair networks running in outdoor locations.

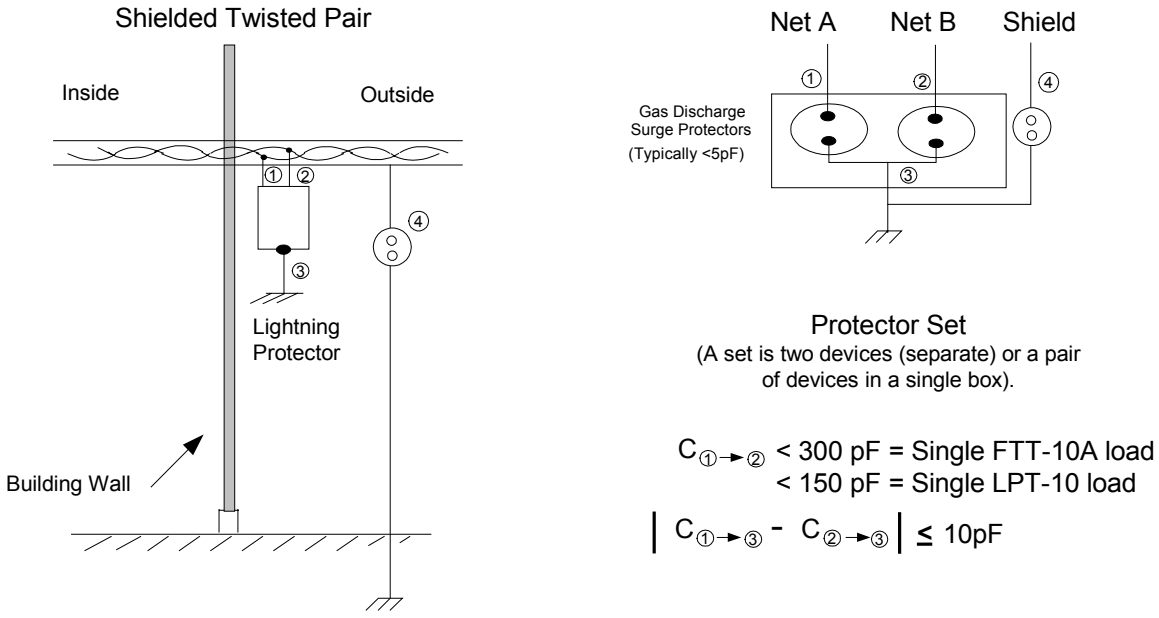


Figure 5.4 Network and Shield Lightning Protection

It is important that **every** FTT-10A node on the network segment, whether located indoors or outdoors, have the protection circuitry described in the Transceiver Pinout section of chapter 2, *Electrical Interface*. Surge protection circuitry must also be used on each LPT-10 link power node. This is *in addition* to any building entrance protection devices present on the network.

Vibration and Mechanical Shock Issues

The FTT-10A transceiver is designed to withstand moderate levels of vibration and mechanical shock while operating. Echelon has tested the FTT-10A transceiver operating in typical two-layer application boards to verify that the transceiver can withstand occasional vibration levels up to 1.5g peak-to-peak over the frequency range of 8Hz to 2kHz (where one "g" = 9.8m/s^2), and occasional mechanical shocks up to 100g.

EN 61000-4 Electromagnetic Compatibility (EMC) Testing

Echelon has tested the FTT-10A transceiver operating in typical two-layer application boards to verify that the transceiver complies with the five applicable EN 61000-4 test requirements (formerly known as IEC 1000-4 tests). Provided that a node's PCB is designed following the guidelines in chapter 2, the FTT-10A transceiver should pass the EN 61000-4 tests described in table 5.1.

Table 5.1 EN 61000-4 Test Immunity Levels

EN Test	***Description***	***FTT-10A Immunity Level***
EN 61000-4-2	ESD	Level 4
EN 61000-4-3	Radiated Susceptibility	Level 3
EN 61000-4-4	Burst	Level 4
EN 61000-4-5	Surge	Level 3
EN 61000-4-6	Conducted RF Immunity Standard Circuit (figures 2.1-2.2) with Logic ground floating With Common-Mode Choke (see text) Logic ground floating or earth-grounded	 Level 3 Level 3

EN 61000-4-2 ESD testing is performed on a metal test table using an ESD transient generator [13]. Level 4 testing involves injecting up to ±8kV contact discharges and up to ±15kV air discharges into the product under test. Depending on the product design, discharges may be injected at the network connector, power connector and other user-accessible areas. Under the test, proper operation continues with occasional loss of a packet and infrequent node resets.

EN 61000-4-3 RF Susceptibility testing is generally performed in an RF-shielded anechoic chamber[14]. The product under test is placed on a non-conducting table in the chamber, and antennas are used to subject the product to intense radio frequency fields. Under the test, proper operation continues with occasional loss of a packet. Level 2 testing is performed with a field of 3V/m, which is classified by the test standard as a "moderate electromagnetic radiation environment." Level 3 testing is performed with a field of 10V/m, which is classified by the standard as a "severe electromagnetic radiation environment."

EN 61000-4-4 Burst testing is performed on a non-conducting table, with 1 meter of the network cable clamped in a high-voltage burst generation apparatus[15]. Under the test, proper operation continues with occasional loss of a packet. There are three bursts injected onto the network cable each second. Level 3 testing is performed with ±1kV bursts, which are classified by the test standard as representative of a "typical industrial environment." Level 4 testing is performed with ±2kV bursts, which are representative of a "severe industrial environment."

EN 61000-4-5 Surge testing is performed on a non-conducting table using specialized surge generation equipment[16]. The surges are injected directly into the network wiring via a coupling circuit. See figure 10 of EN 61000-4-5 (formerly figure 11 of IEC 801-5). Under the test, proper operation continues with the occasional loss of a

packet. Level 2 testing is performed with up to ±1kV surges, and Level 3 testing is performed with up to ±2kV surges.

For more information on levels and installation classes, see EN 61000-4-5. The applicable surge test levels and coupling mode specified by EN 61000-4-5 can be found in table A.1 of [16] as follows:

- balanced circuits/lines;
- coupling mode is line-to-ground, either polarity;
- surge waveform is 1.2/50μs (8/20μs) combination wave for classes 1-4.

EN 61000-4-6 Conducted RF Immunity testing is performed on a metal test table using an RF signal generator, an RF power amplifier, and specialized "coupling-decoupling" network (CDN) devices[18, 19]. A typical test setup for use with LONWORKS network devices is shown in figure 5.4. The test equipment drives a large common-mode noise voltage onto the twisted pair cable that connects to the Equipment Under Test (EUT). The Auxiliary Equipment (AE) must be able to continue communicating with the EUT during the test. The CRC error rate for this communication should generally be less than 1%, indicating a negligible loss of network functionality. During the test, the RF signal generator is set to an amplitude modulation (AM) depth of 80%, and the frequency is slowly swept from 150kHz to 80MHz. Level 2 testing, which represents a "light industrial environment," is performed with an injected common-mode voltage on the EUT's network cable of 3Vrms (15.3Vp-p including the 80% AM). Level 3 testing, which represents a "harsh industrial environment," is performed with an injected common-mode voltage on the EUT's network cable of 10Vrms (50.9Vp-p including the 80% AM).

Note that the CDN test method is the preferred method according to the EN 61000-4-6 specification. The T2 and S2 CDN models shown in the figures allow FTT-10A network communications to pass through them with negligible signal degradation. Echelon recommends using these CDNs for EN 61000-4-6 testing of FTT-10A transceiver-based devices, rather than using the alternate "Bulk Current Injection" (BCI) technique.

A typical set-up for EN 61000-4-6 testing of an FTT-10A-based node and unshielded twisted pair network wire is shown in the figure 5.5.

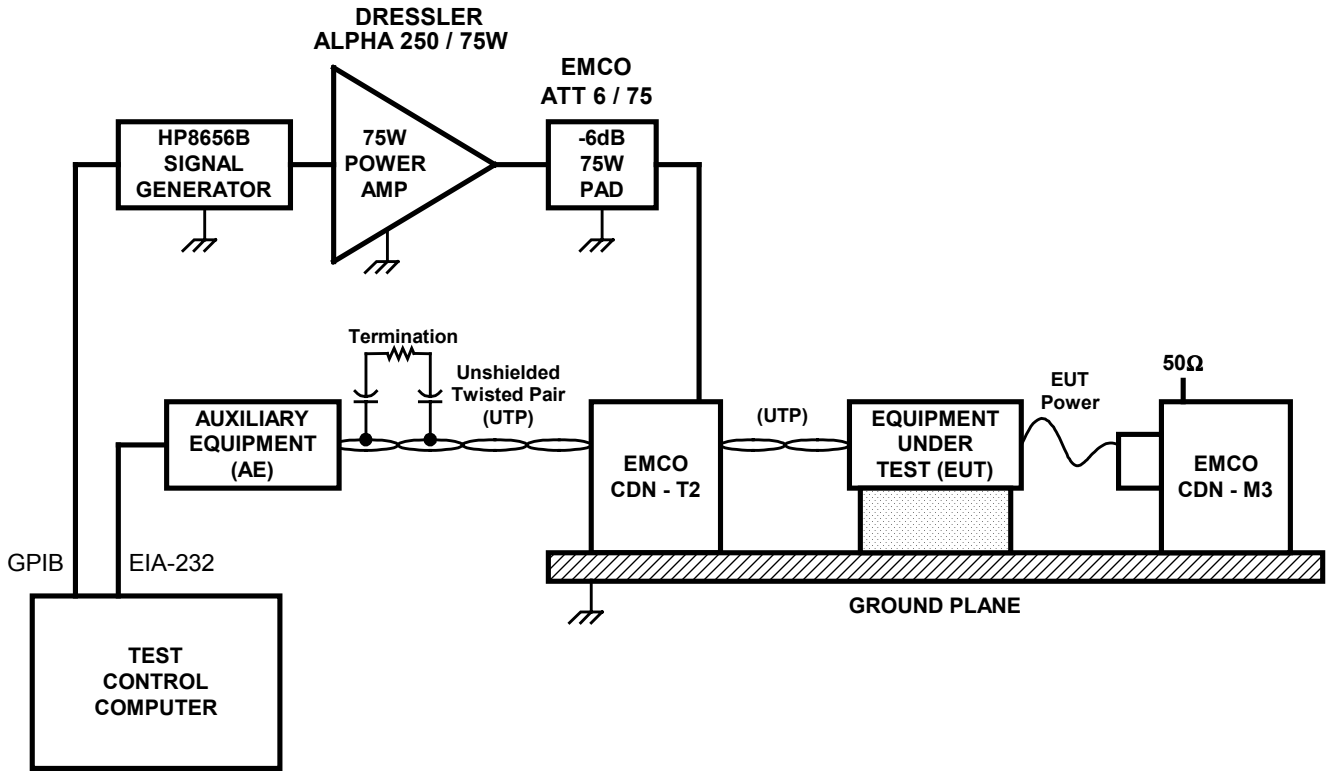


Figure 5.5 Typical EN 61000-4-6 Test Set-up for Unshielded Twisted Pair (UTP)

For the EN 61000-4-6 tests, the EUT is placed on a 10cm high, non-conducting support on top of the metal ground plane. If the EUT's chassis is connected to earth ground in typical installations, then it should be connected directly to the metal ground plane during the EN 61000-4-6 tests via a short wire. If the EUT is left floating in normal use, then there should be no connection between the EUT and earth ground for the EN 61000-4-6 tests. The power connection for the EUT should be routed through a suitable decoupling device, such as a non-driven M3 CDN, as shown in the figure. During the network immunity tests, any I/O lines that come out of the EUT should also pass through a decoupling network. The objective of the T2 CDN in the figure is to drive the large common-mode noise signal into the EUT's network cable, while still isolating the AE unit's network cable from the noise. The M3 CDN in the figure ensures that the power supply input to the EUT is not an RF return path for the purposes of the EN 61000-4-6 test. See the EN 61000-4-6 test standard[18] and related articles[19] for more information about test setups and procedures.

The following figure shows the changes in the EN 61000-4-6 test setup to accommodate shielded twisted pair (STP) networks. An S2 CDN is used instead of the T2 CDN, and the shield should be connected to earth ground as shown in figure 4.7, *Terminating and Grounding Shielded Twisted Pair Cable*.

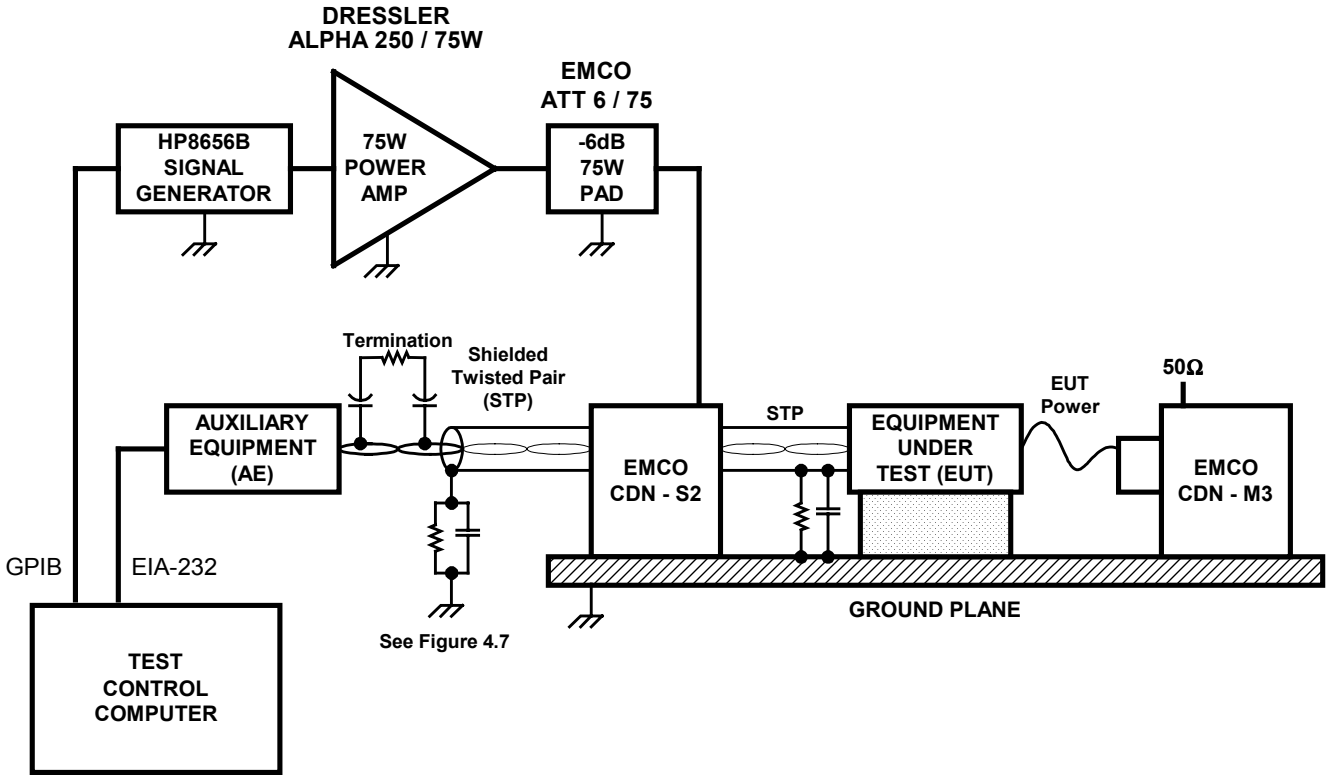


Figure 5.6 Typical EN 61000-4-6 Test Set-up for Shielded Twisted Pair (STP)

As indicated in table 5.1, FTT-10A-based nodes will generally pass the higher 10Vrms (50.9Vpp) test level with little or no interference with data communications, as long as the logic ground for the device is floating with respect to external earth ground. For example, Echelon's LonPoint® devices do not generally have a direct connection between their internal logic ground and external earth ground, and pass the 10Vrms test level.

When an FTT-10A-based node has a local connection between its logic ground and external earth ground, then either a common-mode isolation choke or shielded twisted pair network cabling will generally be needed in order to pass the 3Vrms or 10Vrms test level of EN 61000-4-6. Figure 5.7 shows the CM noise immunity of the FTT-10A with and without the Network Isolation choke per 1000-4-6. Figure 5.8 shows the measurement method for determining the common mode noise on a network. Note the two 1KΩ resistors limit the bandwidth of the measurement by approximately 50MHz. The specification for an appropriate common-mode isolation choke is given in Appendix F. When shielded twisted pair cable is used for immunity to EN 61000-4-6 testing, the shield must be connected to earth ground at the EUT's network cable connection. This connection should be made as shown in figure 4.7, *Terminating and Grounding Shielded Twisted Pair Cable*.

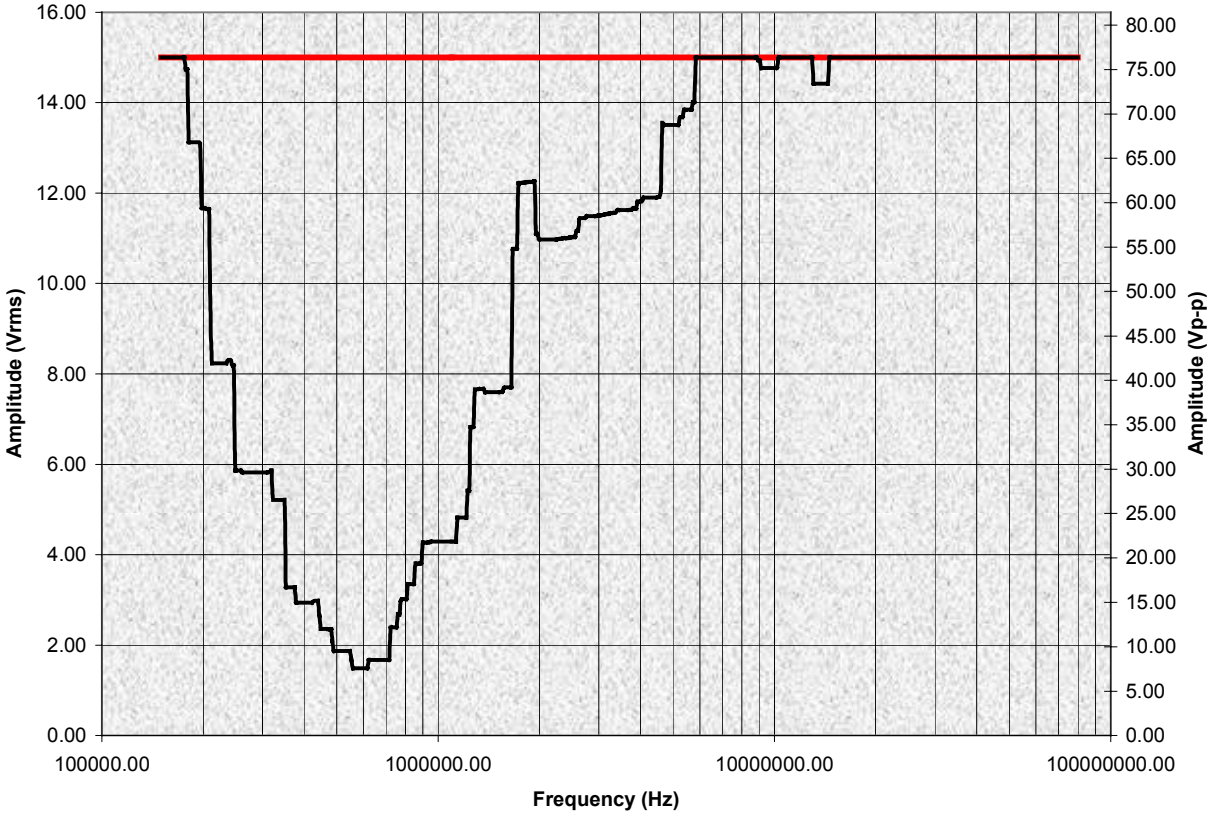


Figure 5.7 FTT-10A Common-Mode Noise Immunity

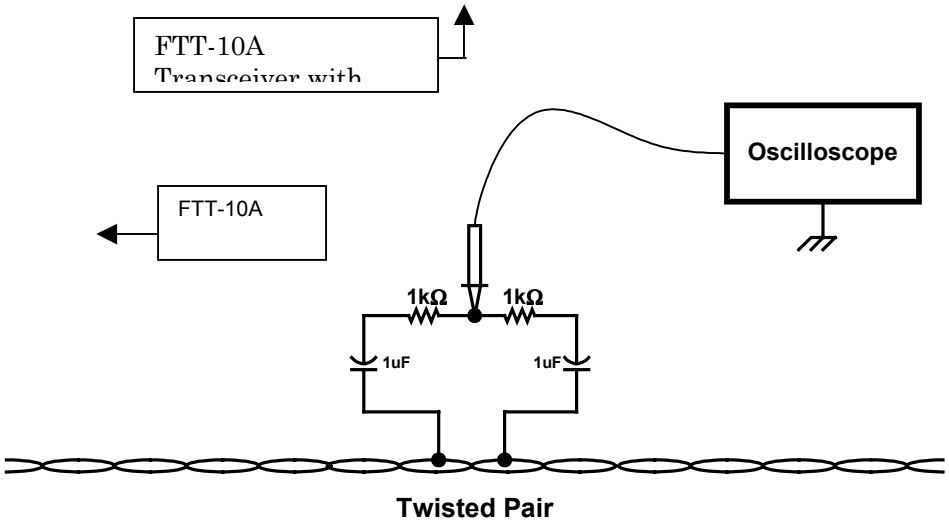


Figure 5.8 Common-Mode Noise Measurement Method

6
Programming Considerations

This section explains the integration of the FTT-10A Free Topology Transceiver using the LonBuilder Developer's Workbench and NodeBuilder Development Tool. It covers considerations relating to channel definition and custom node image generation.

Application Program Development and Export

Application programs are initially developed, tested, and debugged using the LonBuilder Developer's Workbench or the NodeBuilder® Development tool. See the *LonBuilder User's Guide* and *NodeBuilder User's Guide* for detailed instructions on developing and testing applications. Actual unit and system testing on the TP/FT-10 channel requires one or more Echelon Model 77040 FTM-10 SMX™ Standard Modular Transceivers. The following two sections describe specifics related to each development environment.

LonBuilder Developer's Workbench

The ideal development environment connects all LonBuilder processor cards to the TP/FT-10 twisted pair channel to enable system test and protocol analysis of the functioning control network under test. The FTM-10 attaches to LonBuilder processor cards using the Echelon Model number 27100 SMX Adapter mounted on the transceiver expansion connectors. Refer to the *LonBuilder Hardware Guide*[1] and *LONWORKS SMX Transceiver Installation Instructions*[9] for detailed instructions on installing the SMX adapter and FTM-10 transceiver.

Warning: A common mistake is to forget to reposition the backplane transceiver jumpers on the LonBuilder processor card to the *External Transceiver* setting prior to installing the SMX adapter. Also, confirm jumper settings for the FTM-10 transceiver prior to installing on the SMX adapter.

LonBuilder configures the Neuron Chip communications port according to the channel definitions accessed by pressing the `Network` and `Channel` buttons of the LonBuilder Navigator. Create a TP/FT-10 channel definition to use the `TP/FT-10` as the `Std Xcvr Type` with the `Enforce Std Type` option set to `Yes`. The `TP/FT-10` transceiver parameters are compatible with the FTT-10, FTT-10A, and LPT-10 transceivers. Versions of LonBuilder prior to release 3.0 do not include the standard transceiver definition for `TP/FT-10`. The standard transceiver definition is listed in table 6.2.

Application development begins by properly specifying the hardware characteristics of the system under development. Table 6.1 shows the hardware properties for a typical FTT-10A-based custom node. Assigning these properties to a LonBuilder emulator for execution will allow the developer to test the application performance at the true clock rate of the custom node that will eventually host the application. The emulator can also take on the memory map of the Neuron 3120 Chip by changing the hardware property `Neuron Chip` model number to 3120. The backplane network in the LonBuilder Development Station can approximate the performance of the FTT-10A transceiver by creating a `Channel` with `TP/FT-10` selected as the transceiver type, setting `Enforce Std type` to '`No`' and changing the `Comm Mode` type to `Differential`.

Two or more FTT-10A transceivers can function as a physical layer repeater to extend the size of the network. The standard channel definition shown in table 6.2 accommodates the delay that occurs as a packet is forwarded by a single physical layer repeater. Only one physical layer repeater should be placed in series between any two nodes on a channel. If additional cabling or nodes are required, Echelon routers must be used. If additional repeaters were to exist in the path of a packet, the `Rcv Start Delay` and `Missed Pream` parameters for the channel definition would have to be modified according to the notes shown in table 6.2, and the channel would no longer be interoperable. As the number of physical layer repeaters increases, the overall channel capacity is reduced because the inter-packet spacing is increased. In high traffic applications, LONWORKS routers should be used to selectively forward packets. Systems designed using LONWORKS routers instead of physical layer repeaters will have a higher overall network packet capacity. For channels with no repeaters, channel performance can be improved by adjusting these parameters with N= 0, however, the channel will no longer be interoperable. **Note: Use the standard channel definition in order to achieve LONMARK interoperability.**

The LonBuilder Developer's Workbench is initially used to develop and debug applications on emulators. Once application testing on the emulators is completed, the LonBuilder software is used to generate custom system images for the actual target hardware (see the *LonBuilder User's Guide*, Chapter 7, and the Echelon Engineering Bulletin *LONWORKS Custom Node Development*).

A LonBuilder Router with a LonBuilder SMX Adapter and FTM-10 Modular Transceiver also may be used to interface the LonBuilder hardware to a TP/FT-10 channel. This configuration is useful when multiple transceivers types are present in the system. When changing the LonBuilder hardware configuration to attach a LonBuilder router to a TP/FT-10 channel, ensure the following steps are completed:

- Select a backplane channel for side A and a TP/FT-10 channel for side B in the LonBuilder Router `Target HW` definition;
- Ensure that channel A of the router is connected to the backplane channel. For level 1 and 2 routers, a backplane transceiver must be installed in the router P2 channel A transceiver expansion connector. For level 3 routers, JP1 *must* be in the "B" position;
- Mount an FTM-10 Modular Transceiver on a LonBuilder SMX Adapter;
- Mount the LonBuilder SMX Adapter on the router P3 channel B transceiver expansion connector. For level 3 routers, JP2 *must* be in the "A" position;
- Create a router node specification for the LonBuilder Router;
- Use the LonBuilder tool to install and load/start the router.

A heavily loaded TP/FT-10 channel may generate more traffic than can be forwarded through the LonBuilder Router. This may cause the LonBuilder Protocol Analyzer to miss some of the packets on the TP/FT-10 channel. To ensure that the protocol analyzer receives all packets, it must be directly attached to the TP/FT-10 channel. This allows the protocol analyzer to monitor all channel traffic. When changing the LonBuilder hardware configuration to attach the protocol analyzer to the TP/FT-10 channel, ensure that the following steps are completed:

- Select a TP/FT-10 channel in the protocol analyzer `Network Mgmt.Target HW` definition;
- Mount an FTM-10 Modular Transceiver on a LonBuilder SMX Adapter;
- Mount the LonBuilder SMX Adapter on the control processor P3 protocol analyzer transceiver expansion connector. For level 3 control processors, JP1 *must* be in the "A" position;
- Use the LonBuilder software to install the protocol analyzer.

Refer to the custom node section of Chapter 7 of the *LonBuilder User's Guide* to best understand the migration of the application from emulators to actual FTT-10A-based custom nodes.

Warning: In custom designs using Flash memory, the programmed device must be explicitly secured by the PROM programmer once the image is programmed. See Software Data Protection (SDP) information provided by the manufacturer of the PROM programmer.

Warning: All Neuron 3120 Chips must be programmed with the generated .NEI image before they are soldered in a PCB assembly.

Table 6.1 A Typical Hardware Property Record for an FTT-10A Custom Node

HW Property Name	5MHz_3150	*User's choice*
Neuron Chip	3150	
Input Clock Rate	5 MHz	
ROM Size	128 pages	*64 for network downloads*
EEPROM Size	0	
RAM Size	0	

Table 6.2. Standard LPT-10 and FTT-10A Channel Definition for both Bus and Free Topologies

Variable	***TP/FT-10 Standard Transceiver Type***
Comm Mode	Single-ended (see note 4)
Comm Rate	78.13kbps
Min Clock Rate	5MHz
Num Priorities	4
Osc Accuracy	200ppm
Osc Wakeup	0µsec
Avg Packet Size	15 bytes
Collision Detect	No
CD terminate after preamble	No

CD through packet end	No
Bit Sync Threshold	4.0 bits
Rcv Start Delay	9.0 bits (see note 2)
Rcv End Delay	0.0 bits
Indeterm Time	24.0 bits
Min Interpacket Time	0.0 bits
Turnaround	0 µsec
Missed Pream	4.0 bits (see note 3)
Use Raw Data?	No

Notes:

1. For the Following, "N" must be 1 for the interoperable LONMARK TP/FT-10 channels.
2. For N repeaters in a packet path: Rcv Start Delay = 4.5 * (N + 1) bits.
3. For N repeaters in a packet path: Missed Pream = 2.0 * (N + 1) bits.
4. Use Differential mode when emulating a TP/FT-10 channel on the LonBuilder backplane.

NodeBuilder Development Tool

The NodeBuilder development tool must be configured to use the TP/FT-10 channel by installing FTM-10 SMX transceivers on both the PCNSS card and the LTM-10 target. Initial device development is done using the LTMRAM.DTM device template to target the LTM-10 for the execution environment. NodeBuilder development tool users must be aware that the LTM-10 has a 10MHz input clock. If the hardware will run at a lower input clock rate, the design of the application must be tolerant of the reduced execution performance.

Once the application has been developed, tested, and debugged on the LTM-10 target, a device template must be generated to match the final target hardware. Success in generating the ROM image for the final custom hardware requires careful attention to the device template definition. Follow these steps and refer to chapter 5 of the *NodeBuilder User's Guide*[5] and *LONWORKS SMX Transceiver Installation Instructions*[9].

1. Open the Device Template editor by pressing the `Edit` button for the `Device Template frame` in the `General` tab of the `Device` window.
2. Carefully specify all fields for each tab in the Device Template editor for the target hardware. Table 6.3 shows an example device template for the Echelon Model 55030-01 TP/FT-10 control module. Common errors which must be avoided include: Clock Speed mismatches the hardware, the Transceiver Type is not selected, Neuron Chip model is not properly specified, Flash based modules specify the wrong Flash sector size.
3. Select `File, Save As..` from the NodeBuilder menu to save the template file.

4. Check that the newly defined template file is shown in the `Device Template Frame` of the Device Window `general tab dialog box`.

5. Select `Build, Build` from the NodeBuilder menu to generate the necessary images to program your custom device. Building and Loading the Application Image in chapter 5 of the *NodeBuilder User's Guide* contains a table which describes the extensions applied to the various images created when a build occurs. Take the appropriate image to a PROM programmer and generate the initial PROM or Flash image.

Warning: Flash memory must be explicitly secured by the PROM programmer once the image is programmed. See SDP information provided by the manufacturer of the PROM programmer.

Warning: All Neuron 3120 Chips must be programmed with the generated .NEI image before they are soldered onto a PCB assembly.

Table 6.3. Example NodeBuilder Device Template Values for a TP/FT-10 Control Module

Hardware				
	Target Hardware:	Other		
	Neuron Model:	3150		
	Clock Speed:	5MHz		
	Transceiver Type:	TP/FT-10		
Firmware				
	System Image:	Default		
	Version:	6		
	Image Name:	SYS3150		
Memory Map			Start Address	End Address:
	ROM:	128	0000	7FFF
	NV RAM:	0	0000	0000
	RAM:	0	0000	0000
	I/O:	0	0000	0000
	Memory Type:			

7

References

This section provides a list of the reference material used in the preparation of this manual.

Reference Documentation

[1] *LonBuilder Hardware Guide*, part number 078-0003-01, Echelon Corporation, 1995.

[2] *Neuron Chip Data Book* as published by Cypress.

[3] *Neuron Chip Data Book* as published by Toshiba.

[4] *LONWORKS Custom Node Development* engineering bulletin, part number 005-0024-01, Echelon Corporation, 1995.

[5] *NodeBuilder User's Guide*, part number 078-0141-01, Echelon Corporation, 1995.

[6] 47CFR15, Subpart B (Unintentional Radiators), *U.S. Code of Federal Regulations*, (formerly known as FCC Part 15, Subpart J).

[7] (deleted)

[8] *EN 55022, Emissions Limits for Information Technology Equipment* (based on CISPR 22).

[9] *LONWORKS SMX Transceiver Installation Instructions,* 078-0145-01, Echelon Corporation, 1999.

[10] *Protection of Electronic Circuits from Overvoltages*, by Ronald B. Standler, John Wiley & Sons, 1989.

[11] *Noise Reduction Techniques in Electronic Systems*, 2nd ed., by Henry W. Ott, John Wiley & Sons, 1988.

[12] "ESD as an EMI Problem...How to Prevent and Fix," *EDN Designer's Guide to Electromagnetic Compatibility*, EDN Supplement, pp. S23-S29, 1/20/94.

[13] *EN 61000-4-2:1995,* Section 4.2: "Electrostatic discharge immunity test".

[14] *EN 61000-4-3:1997,* Part 4, Section 3: "Radiated, radio-frequency electromagnetic field immunity test".

[15] *EN 61000-4-4:1995,* Part 4, Section 4: "Electrical fast transient / burst immunity test".

[16] *EN 61000-4-5:1995,* Part 4, Section 5: "Surge immunity test".

[17] *Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks,* 005-0023-01, Echelon Corporation, 1999.

[18] *EN 61000-4-6:1996,* Part 4, Section 6: "Immunity to conducted disturbances, induced by radio-frequency fields".

[19] "How to test for conducted immunity," by Paul Phillips, *Approval Magazine*, March/April 1999.

Appendix A

Guidelines for FTT-10 Users

This appendix contains information on converting an existing design from the FTT-10 to the FTT-10A transceiver. Also included are EMI test results comparing devices using the FTT-10 and FTT-10A transceiver operating at both 5MHz and 10MHz.

Mechanical Differences

The FTT-10A transceiver is an encapsulated assembly whereas the FTT-10 transceiver has open frame construction. Table A.1 compares mechanical dimensions of the FTT-10 and FTT-10A transceivers. As shown in figure A.1, the FTT-10A transceiver is roughly half the height of the FTT-10 transceiver and slightly smaller in width. The maximum length of both products is identical, however, the pin grid is shifted a bit with respect to the shorter edges as illustrated in figure A.2. The edge common to the NET_A and NET_B pins extends farther in the FTT-10A transceiver than in the FTT-10 transceiver. If the FTT-10A transceiver is placed on a PC board designed for the FTT-10 transceiver, there may be mechanical interference with components located adjacent to the NET_A/ NET_B edge of the FTT-10A transceiver.

Table A.1 Mechanical Dimensions Comparison

	mm		inches	
	FTT-10	FTT-10A	FTT-10	FTT-10A
Height maximum	14.1	7.2	0.56	0.28
Width maximum	15.2	13.7	0.60	0.54
Length maximum	17.8	17.8	0.70	0.70
Datum to NET_A/ NET_B Edge				
nominal	15.1	15.7	0.59	0.62
maximum	not specified	16.2	not specified	0.64

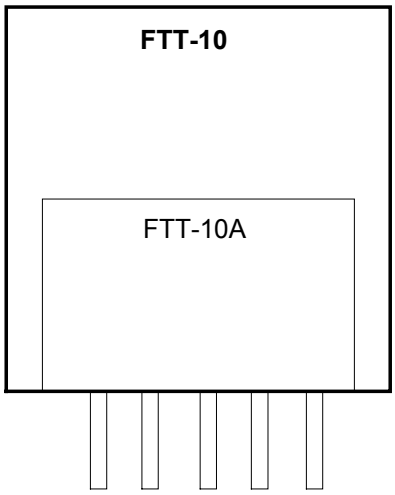


Figure A.1 End View Comparison

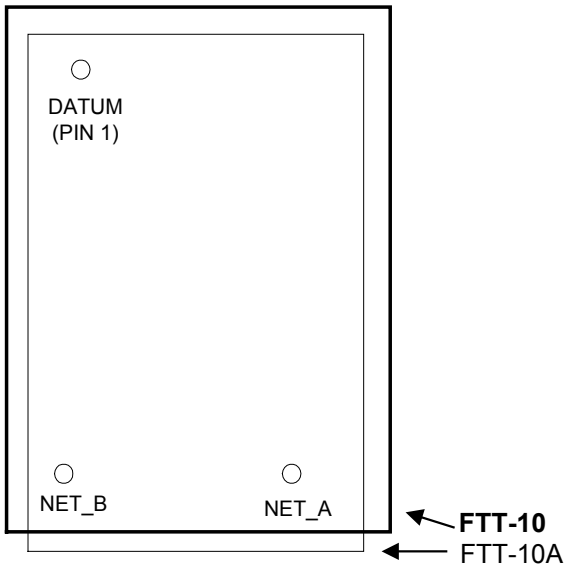


Figure A.2 Top View Comparison

Pinout & External Circuit Differences

The FTT-10A transceiver has a number of built-in functions resulting in fewer pins and simpler external circuitry than the FTT-10 transceiver. Simplification of external circuitry has been qualified with a layout optimized for the FTT-10A transceiver as documented in chapter 2 of this user's guide. For information on existing PC board designs, see the following section.

FTT-10A Pin	***FTT-10 Pin***	***Changes in Pin Function in the FTT-10A Transceiver***
1 VCC	1 VCC	None
2 NET_B	5 NET_B	None
3 NET_A	6 NET_A	None
4 RxD	7 RxD	None
5 TXD	8 TXD/ CLKSEL1	The clock select function is multiplexed with the TXD pin in the FTT-10 transceiver and the CLKSEL1 pin been eliminated due to automatic input clock detection. The TXD pin remains without the CLKSEL1 function. To prevent a possible, brief transient on the network when the Neuron Chip goes through its reset process, the 47kohm CLKSEL1 resistor R1 as defined in the *LONWORKS FTT-10 Free Topology Transceiver User's Guide* figure 2.1 must be removed.
6 CLK	10 CLK	None
7 T1	11 T1	None
8 GND	12 GND	None
9 T2	13 T2	None
No pin	9 RESET	The FTT-10A transceiver has built-in reset function and therefore has no reset pin. This eliminates the need for pulse-stretching LVI and RC circuitry required by the FTT-10 transceiver. An LVI, if used, should be selected based on Neuron Chip and application electronics requirements.
No pin	3 CLKSEL0	The FTT-10A transceiver automatically detects the frequency of the incoming clock and configures itself accordingly. The FTT-10A transceiver has no CLKSEL0 pin.
No pin	4 TXEN	The FTT-10A transceiver uses activity on TXD to determine when to enable transmission, and accordingly has no TXEN pin. Applications that require a transmit indicator LED can continue to use a buffered CP2 signal.
No pin	2 RX_ACTIVE	The FTT-10A transceiver uses activity on TXD to determine when to enable transmission in a repeater configuration, and accordingly has no RX_ACTIVE pin. Applications that require a received indication LED can use a buffered RXD signal.

Replacement in Existing PC Board Designs

In general, the FTT-10A transceiver may be used in place of the FTT-10 transceiver in any node design, provided that it is done in accordance with the LONWORKS FTT-10 Free Topology Transceiver User's Guide. Echelon has conducted a variety of tests on a typical node using a 2-layer PC board originally designed for the FTT-10, with the FTT-10A transceiver replacing the FTT-10 transceiver. These tests include radiated emissions and IEC 1000-4-2, 1000-4-3, 1000-4-4, and 1000-4-5 (formerly IEC 801-2, 3, 4, and 5) tests described in the user's guide. The FTT-10A transceiver performed as well as, or better than, the FTT-10 transceiver in all tests. Like the FTT-10 transceiver, the FTT-10A transceiver is a component rather than a system, and users should choose an appropriate qualification plan for designs incorporating the FTT-10A transceiver based on specific system requirements.

There are certain cases where the FTT-10A transceiver will require changes to a PC board designed for the FTT-10 transceiver:

As documented above, if the FTT-10A transceiver is placed on a PC board designed for the FTT-10 transceiver, there may be mechanical interference with components located adjacent to the NET_A/ NET_B edge of the FTT-10A transceiver.

The FTT-10A transceiver cannot be used as a physical layer repeater using schematics from the *LONWORKS FTT-10 Free Topology Transceiver User's Guide*. It is very important to use *only* the repeater schematics shown Chapter 2 of this FTT-10A User's Guide. In particular, note that the FTT-10A repeater uses a 5MHz rather than a 2.5MHz clock source, that there is no logical inversion in the path between RXD and TXD signals, and that the external circuitry immediately around the transceiver is somewhat different.

EXTERNAL COMPONENT REMOVAL FROM AN EXISTING BOARD LAYOUT

1. To prevent a possible, brief transient on the network when the Neuron Chip goes through its reset process, the 47kΩ CLKSEL1 resistor (R1 in the *LONWORKS FTT-10 Free Topology Transceiver User's Guide* figure 2.1) should be removed.
2. The following components can be removed from an existing PC board for simplification: Rr, C4, and C5. The LVI may be removed if not required by a Neuron Chip or the application circuitry.

EMI Comparison Scans for the FTT-10 and FTT-10A Transceivers

This section presents EMI scans of both the FTT-10 and FTT-10A transceivers. EMI test data for Echelon's SLTA-10 Serial LonTalk Adapter which utilizes an FTT-10A transceiver operating at10MHz is also presented.

The net result is that devices using the FTT-10 and FTT-10A transceivers have comparable EMI performance, and products using the FTT-10A

transceiver at both 5MHz and 10MHz have been demonstrated to comply with both FCC-B and EN 55022-B limits with margin.

Comparison of FTT-10 and FTT-10A Radiated EMI

A typical test setup was scanned at an outdoor EMI test facility in order to compare radiated emissions from the FTT-10 and FTT-10A transceivers. The test setup is shown in figure A.3.

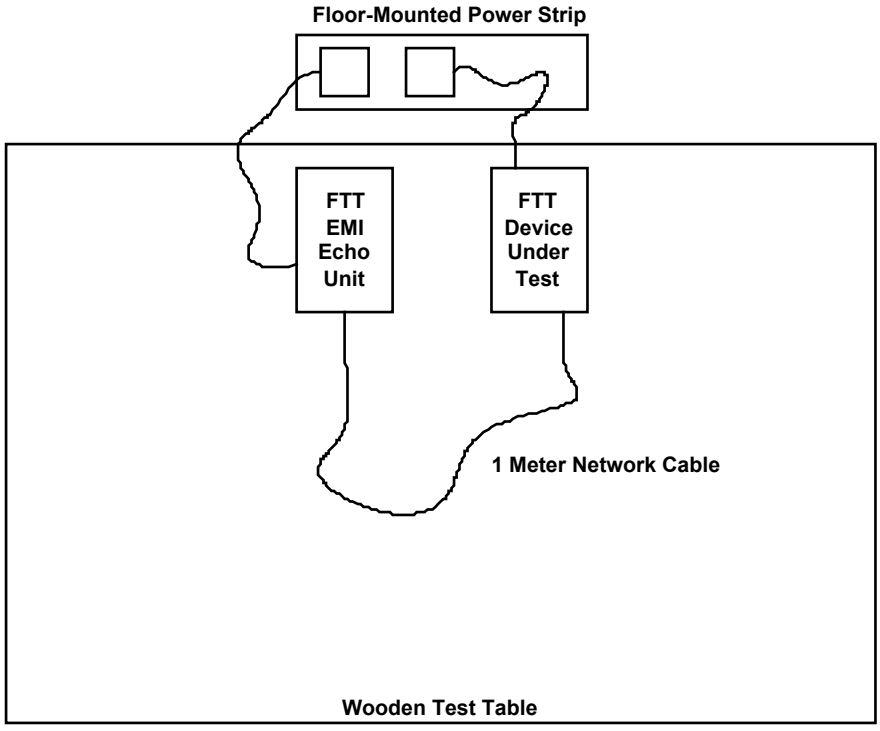


Figure A.3 Test Setup for EMI Comparison of FTT-10 and FTT-10A Transceivers (Top View)

The "FTT EMI Echo Unit" contains a 5MHz Neuron 3120 Chip and an FTT-10 transceiver on a 2-layer PCB. The layout of this PCB is identical to that shown in chapter 2 of the *FTT-10 Free Topology Transceiver User's Guide*. The Echo Unit contains no ferrites or other EMI suppression devices in the network connection. The Neuron Chip in the Echo Unit runs a Neuron C program which continuously queries the status of the Device Under Test.

The "FTT Device Under Test" (DUT) is based on the Echelon's LONWORKS Router. A single control module is placed into the router to serve as the test unit: a production TP/FT-10 control module was used for the 5MHz FTT-10 baseline scans; an FTT-10A transceiver in a production TP/FT-10 control module was used for the 5MHz scans; and an FTT-10A control module (not a production product) was used for the 10MHz FTT-10A scans.

The FTT-10A control module PCB design followed the layout guidelines shown in chapter 2 of this user's guide.

No ferrites or other EMI suppression devices were placed in line with the network connection. The Neuron Chip in the control modules was programmed to rapidly transmit short-length explicit messages. The network traffic level was about 80 packets per second when the DUT was running at 5MHz, and about 140 packets per second when the DUT was running at 10MHz. There were approximately 1 or 2 collisions per second between the DUT and the Echo Unit.

The radiated EMI comparison scans were performed at both 3m and 10m test distances. The 3m test distance (as measured from the test table to the receiving antenna) is used to assess compliance with FCC requirements, while the 10m test is used to assess compliance with EN 55022 requirements. The ANSI C63.4 test procedure was used for all of the test scans.

The results of the comparison scans are shown in figure A.4 and A.5. Figure A.4 shows the results of the comparison scans performed with the test antenna placed 3m away from the test table. Both the FTT-10 and FTT-10A transceivers demonstrate compliance with the FCC-B limit with margin. Figure A.6 shows the results of the comparison scans performed with the test antenna placed 10m away from the test table. Both the FTT-10 and FTT-10A transceivers demonstrate compliance with the EN 55022-B limit with margin.

Figure A.5 also contains test data for the SLTA-10 adapter operating at 10MHz. The SLTA-10 adapter test results are discussed in the next section.

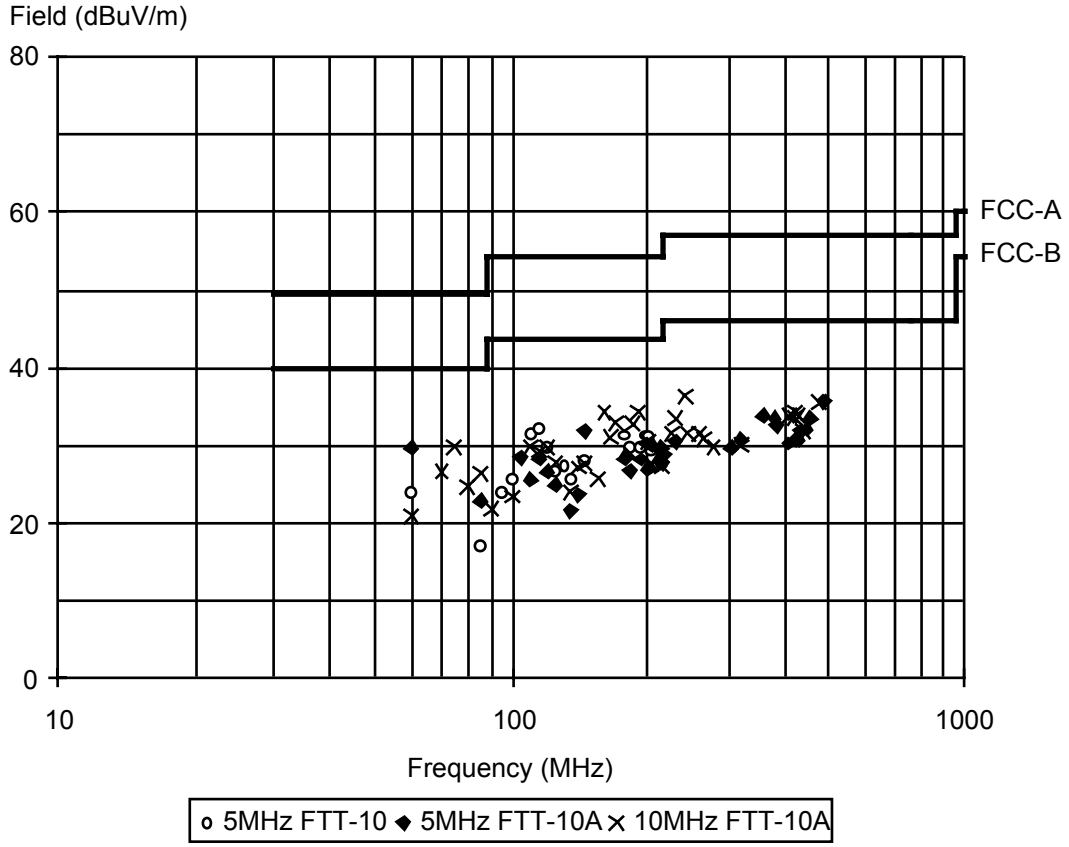


Figure A.4 EMI Scan Data at 3m Test Distance for FCC-B Compliance

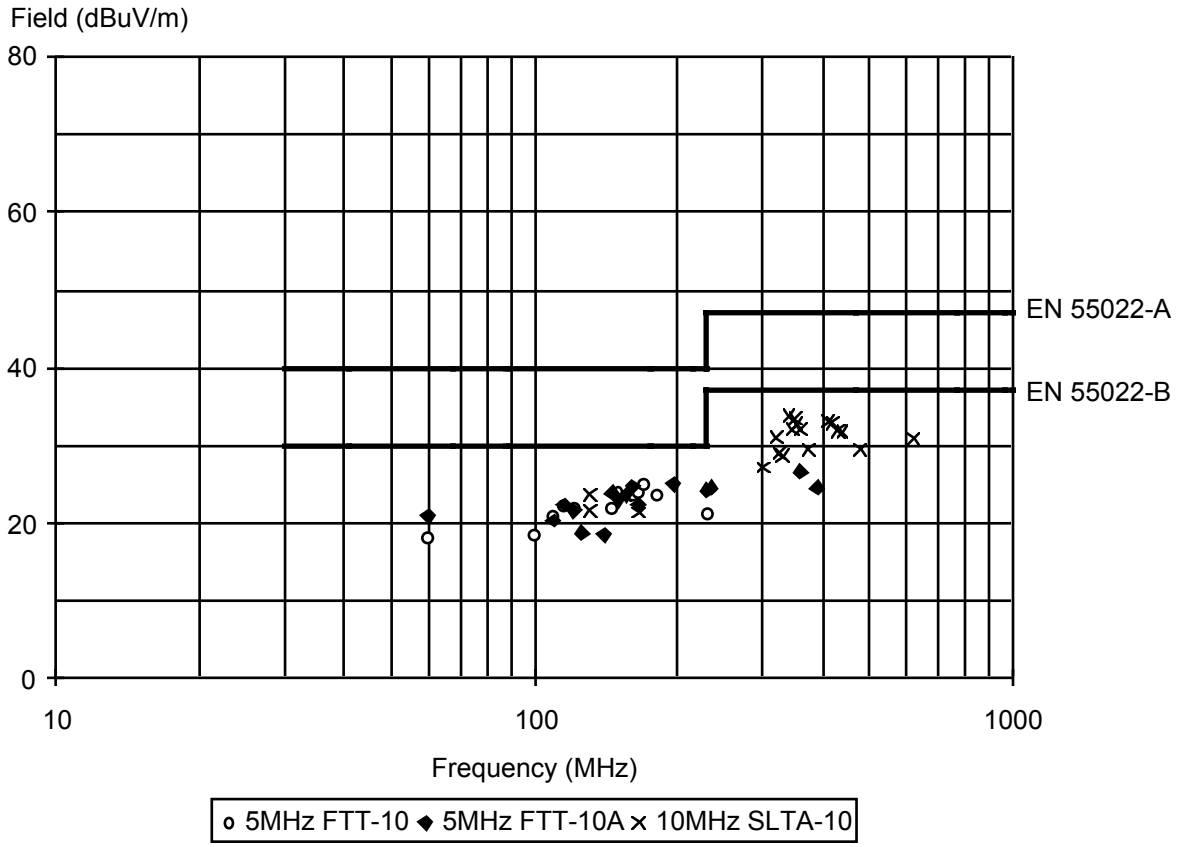


Figure A.5 EMI Scan Data at 10m Test Distance for EN 55022-B SLTA-10

SLTA-10 Adapter EN 55022-B Test Scan

Figure A.5 includes EMI test results for Echelon's SLTA-10 adapters operating at 10MHz with FTT-10A transceivers. The SLTA-10 adapter is representative of a moderately complex end product: in addition to a Neuron 3150 Chip operating at 10MHz, the adapter contains RAM, ROM, programmable logic, a UART, and a switching power supply. The adapter was operated without its common-mode ferrite choke in line with the network connector in order to assess the node emissions without such a choke, which decreases emissions but adds cost. The EMI test setup for the SLTA-10 adapter testing is shown in figure A.6.

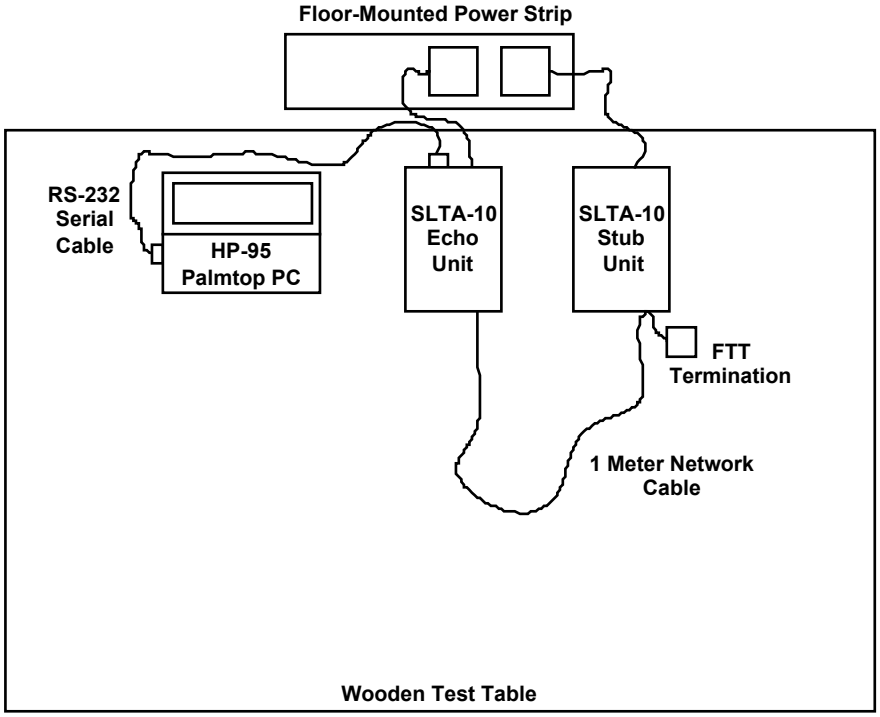


Figure A.6 Test Setup for EMI Scan of theSLTA-10 Adapters (Top View)

The SLTA-10 test setup included two SLTA-10 adapters, each with an FTT-10A transceiver operating at 10MHz. The setup used an HP-95 palmtop PC to send serial RS-232 data to the Echo Unit, and the data were sent via the FTT-10A network to the Stub Unit. The Stub Unit returned the data back to the Echo Unit, which then sent the data back to the PC via the RS-232 serial cable. The returned data pattern was checked for accuracy by the PC, and the process was then repeated.

The results of the10m EMI scan are plotted together with the 5MHz FTT-10A transceiver comparison scans in figure A.6. The 5MHz FTT-10, 5MHz FTT-10A, and 10MHz SLTA-10 test setup all demonstrate compliance with the EN 55022-B limit with margin.

Appendix B

FTT-10A Transceiver-Based Node Checklist

This appendix includes a checklist to ensure that products using the FTT-10A transceiver meet the specifications presented in this user's guide.

FTT-10A Transceiver-based Node Checklist

FTT-10A Transceiver and Neuron Chip Connections

Item	*Check When Completed*	*Description*
1		Transceiver pins connected as shown in table 2.1.
2		Environmental and electrical specifications shown in table 2.2.
3		CLK2 from Neuron Chip connected via trace ≤2cm (0.8").
4		The recommended number and placement of 0.1µF bypass capacitors are near the Neuron Chip. See the *Neuron Chip Data Book* from Toshiba, Motorola, or Cypress, as appropriate.
5		The Neuron Chip and transceiver input clock frequency is ≥5MHz and accurate to at least ± 200 ppm.
6		CP2 and CP3 from the Neuron Chip are not connected to the transceiver.
7		CP4 from the Neuron Chip is connected to VCC
8		The transceiver ground pin is connected to node ground, with low-impedance traces, using a star pattern to a central ground point.
9		The Neuron Chip and transceiver are placed adjacent to one another on the same printed circuit board.
10		If required, a Low Voltage Interrupt (LVI) circuit with open collector output (such as the Motorola MC33064) is used to supply a reset signal to the Neuron Chip.
11		CLK2 guarded by ground traces.
12		Spark gaps, clamping diodes, and 1000 pF 2kV snubbing capacitors are used if air-discharge ESD requirements are applicable.
13		Differential probe measurement between FTT-10A pins T1 and T2 is less than 15mV p-p during periods with no packet activity (see Appendix D for details).

FTT-10A PCB Layout

Item	*Check When Completed*	*Description*
14		Star ground configuration used.
15		Keepout areas observed for PCB.
16		D1/D2 clamp diodes in place with the correct value.
17		Ground planes or wide traces used to lower inductance of the ground system.
18		Vcc routed to the transceiver via a narrow trace ≤0.3mm (0.012") width.
19		C1 placed immediately next to the transceiver.
20		Transceiver ground pin connected to center of star ground via wide and short trace.
21		The “leakage” capacitance from high frequency circuit traces is controlled via guard traces.
22		The product's package is designed to minimize the possibility of ESD hits arcing into the node's circuit board. If the product's package is plastic, then the PCB is supported in the package so that unprotected circuitry on the PCB is not adjacent to any seams in the package. The PCB is not touching the plastic enclosure near a seam.
23		Explicit clamping of user-accessible circuitry is used to shunt ESD currents from that circuitry to the center of the star ground on the PCB.
24		The connector, diodes and decoupling capacitor are all located close to the center of the star ground.
25		Switching power supplies are at least 7.5cm (3 inches) away from the FTT-10A.

FTT-10A Transceiver Programming

Item	*Check When Completed*	*Description*
26		The correct standard transceiver type is defined for the transceiver.

FTT-10A Transceiver Power Supply - General

Item	*Check When Completed*	*Description*
27		Supply provides 4.75VDC minimum, 5.25VDC maximum.

FTT-10A Physical Layer Repeater

Item	*Check When Completed*	*Description*
28		5MHz clock source used.
29		Clock source provides CMOS output level, 200ppm total accuracy, and 60/40 duty cycle.
30		OR gate provides CMOS output and 100nsec maximum propagation dealy.
31		Resistors R1, R2 and capacitor C5 are included.
32		Operating temperature range of repeater is 0 to +85°C (see figure 2.6) or –40 to +85°C (see figure 2.8).
33		When multiple FTT-10A transceivers are used, each transceiver is separated by at least 2.5cm (1 inch) from every other FTT-10A transceiver.

Appendix C

JEDEC Files for Repeater PAL

This appendix contains JEDEC files for the repeater design in figure 2-8. Select the appropriate file based on the PAL package type.

Electronic versions of these files are available on the Echelon web site. The files are located www.echelon.com/support/dev_toolbox. From the home page (www.echelon.com) select downloads, then select Miscellaneous from among the Toolbox files.

PAL JEDEC File, DIP Package Type

```
ABEL 6.40 Data I/O Corp.
JEDEC file for: P22V10 V9.0
Created on: Wed Sep 17 15:47:56 1997

6-Way FTT10-A Repeater DIP PAL(1503)17Sept97
*
QP24* QF5828* QV45* F0*
 X0*
NOTE Table of pin names and numbers*
NOTE PINS Clk_5:1 Clk_5_in:2 RXD1:3 RXD2:4 RXD3:5 RXD4:6 RXD5:7
RXD6:8*
NOTE PINS Q12:9 Q11:10 Q10:11 Q7:13 Q6:14 nClk_5_out:23 TXD:17
Ext_Ctr_Rst:15*
NOTE PINS S1:21 S0:22 lastRXDs:16*
NOTE Table of node names and numbers*
NOTE NODES ORed_RXDs:20*
L0044 11111111111111111111111111111111111111111111*
L0088 11111011111111111111111111111111111111111111*
L0440 11111111111111111111111111111111111111111111*
L0484 11111111101111111111111111111111111111111111*
L0528 11111101111111111111111111111111011101111111*
L0572 11111110111111111111111111111111101110101011*
L0616 11111110111111111111111111111111101110111010*
L0924 11111111111111111111111111111111111111111111*
L0968 11111110111111011111111111111111111111111111*
L1012 11111110111011111111111111111111111111111111*
L1056 11111111111011111111111111111111101111111111*
L1100 11111111111011111111111111111111111110111111*
L1496 11111111111111111111111111111111111111111111*
L1540 11111111101110111011101110111011011111111111*
L3652 11111111111111111111111111111111111111111111*
L3696 11111111101110111111111111111111111111111111*
L3740 11111110111111011111111111111111111111111111*
L4312 11111111111111111111111111111111111111111111*
L4356 11111111111111011111111111111111111111111111*
L4884 11111111111111111111111111111111111111111111*
L4928 11111111101111111111111111111111111111111111*
L4972 11111110111111101111111111111110111111111111*
L5016 11111110111111011111111111111101111111111111*
L5808 11101001000011101101*
V0001 0X000000000N00HLLXXXLLXN*
V0002 CX000000000N00HLLXXXLHXN*
V0003 CX000000000N00HLLXXXLHXN*
V0004 0X010000000N10HLHXXXLHXN*
V0005 CX010000000N10LHHXXXHHXN*
V0006 0X000000000N10HHLXXXHHXN*
V0007 CX000000000N10LLLXXXHHXN*
V0008 CX000000000N00LLLXXXHHXN*
V0009 CX000000000N00LLLXXXHHXN*
V0010 CX000000000N00LLLXXXHHXN*
V0011 CX000000000N00LLLXXXHHXN*
V0012 0X010000000N10HLHXXXHHXN*
```

V0013 CX010000000N10LHHXXXHHXN*
V0014 CX010000000N00LHHXXXHHXN*
V0015 CX010000000N00LHHXXXHHXN*
V0016 CX010000000N00LHHXXXHHXN*
V0017 CX010000000N00LHHXXXHHXN*
V0018 0X000000000N10HHLXXXHHXN*
V0019 CX000000000N10LLLXXXHHXN*
V0020 CX000000000N00LLLXXXHHXN*
V0021 CX000000000N00LLLXXXHHXN*
V0022 CX000000000N00LLLXXXHHXN*
V0023 CX000000000N00LLLXXXHHXN*
V0024 0X010000000N10HLHXXXHHXN*
V0025 CX010000000N10LHHXXXHHXN*
V0026 CX010000000N00LHHXXXHHXN*
V0027 CX010000000N00LHHXXXHHXN*
V0028 CX010000000N00LHHXXXHHXN*
V0029 CX010000000N00LHHXXXHHXN*
V0030 0X000000000N10HHLXXXHHXN*
V0031 CX000000000N10LLLXXXHHXN*
V0032 CX000000000N00LLLXXXHHXN*
V0033 CX000000000N00LLLXXXHHXN*
V0034 CX000000000N00LLLXXXHHXN*
V0035 CX000000000N00LLLXXXHHXN*
V0036 CX000000000N10LLLXXXHHXN*
V0037 CX000000000N11LXLXXXHLXN*
V0038 CX100000001N00LHLXXXHLXN*
V0039 CX010000001N00LHLXXXHLXN*
V0040 CX001000001N00LHLXXXHLXN*
V0041 CX000100011N00LHLXXXHLXN*
V0042 CX000010100N00LHLXXXHLXN*
V0043 CX000001101N11LHLXXXHLXN*
V0044 CX000000110N00HLLXXXLHXN*
V0045 CX000000000N00HLLXXXLHXN*
C7A2B*
□BAD9

PAL JEDEC File, PLCC Package Type

```
ABEL 6.40 Data I/O Corp.
JEDEC file for: P22V10C V9.0
Created on: Wed Sep 17 14:57:47 1997

6-Way FTT10-A Repeater PLCC PAL(1448)17Sept97
*
QP28* QF5828* QV45* F0*
 X0*
NOTE Table of pin names and numbers*
NOTE PINS Clk_5:2 Clk_5_in:3 RXD1:4 RXD2:5 RXD3:6 RXD4:7 RXD5:9
RXD6:10*
NOTE PINS Q12:11 Q11:12 Q10:13 Q7:16 Q6:17 nClk_5_out:27 TXD:20
Ext_Ctr_Rst:18*
NOTE PINS S1:25 S0:26 lastRXDs:19*
NOTE Table of node names and numbers*
NOTE NODES ORed_RXDs:24*
L0044 11111111111111111111111111111111111111111111*
L0088 11111011111111111111111111111111111111111111*
L0440 11111111111111111111111111111111111111111111*
L0484 11111111101111111111111111111111111111111111*
L0528 11111011111111111111111111111111011101111111*
L0572 11111101111111111111111111111111101110101011*
L0616 11111101111111111111111111111111101110111010*
L0924 11111111111111111111111111111111111111111111*
L0968 11111101111110111111111111111111111111111111*
L1012 11111101110111111111111111111111111111111111*
L1056 11111111110111111111111111111111101111111111*
L1100 11111111110111111111111111111111111110111111*
L1496 11111111111111111111111111111111111111111111*
L1540 11111111101110111011101110111011011111111111*
L3652 11111111111111111111111111111111111111111111*
L3696 11111111101110111111111111111111111111111111*
L3740 11111101111110111111111111111111111111111111*
L4312 11111111111111111111111111111111111111111111*
L4356 11111111111111011111111111111111111111111111*
L4884 11111111111111111111111111111111111111111111*
L4928 11111111101111111111111111111111111111111111*
L4972 11111101111111101111111111111110111111111111*
L5016 11111101111111011111111111111101111111111111*
L5808 11101001000011101101*
V0001 N0X0000N00000NN00HLLXNXXLLXN*
V0002 NCX0000N00000NN00HLLXNXXLHXN*
V0003 NCX0000N00000NN00HLLXNXXLHXN*
V0004 N0X0100N00000NN10HLHXNXXLHXN*
V0005 NCX0100N00000NN10LHHXNXXHHXN*
V0006 N0X0000N00000NN10HHLXNXXHHXN*
V0007 NCX0000N00000NN10LLLXNXXHHXN*
V0008 NCX0000N00000NN00LLLXNXXHHXN*
V0009 NCX0000N00000NN00LLLXNXXHHXN*
V0010 NCX0000N00000NN00LLLXNXXHHXN*
V0011 NCX0000N00000NN00LLLXNXXHHXN*
V0012 N0X0100N00000NN10HLHXNXXHHXN*
```

V0013 NCX0100N00000NN10LHHXNXXHHXN*
V0014 NCX0100N00000NN00LHHXNXXHHXN*
V0015 NCX0100N00000NN00LHHXNXXHHXN*
V0016 NCX0100N00000NN00LHHXNXXHHXN*
V0017 NCX0100N00000NN00LHHXNXXHHXN*
V0018 N0X0000N00000NN10HHLXNXXHHXN*
V0019 NCX0000N00000NN10LLLXNXXHHXN*
V0020 NCX0000N00000NN00LLLXNXXHHXN*
V0021 NCX0000N00000NN00LLLXNXXHHXN*
V0022 NCX0000N00000NN00LLLXNXXHHXN*
V0023 NCX0000N00000NN00LLLXNXXHHXN*
V0024 N0X0100N00000NN10HLHXNXXHHXN*
V0025 NCX0100N00000NN10LHHXNXXHHXN*
V0026 NCX0100N00000NN00LHHXNXXHHXN*
V0027 NCX0100N00000NN00LHHXNXXHHXN*
V0028 NCX0100N00000NN00LHHXNXXHHXN*
V0029 NCX0100N00000NN00LHHXNXXHHXN*
V0030 N0X0000N00000NN10HHLXNXXHHXN*
V0031 NCX0000N00000NN10LLLXNXXHHXN*
V0032 NCX0000N00000NN00LLLXNXXHHXN*
V0033 NCX0000N00000NN00LLLXNXXHHXN*
V0034 NCX0000N00000NN00LLLXNXXHHXN*
V0035 NCX0000N00000NN00LLLXNXXHHXN*
V0036 NCX0000N00000NN10LLLXNXXHHXN*
V0037 NCX0000N00000NN11LXLXNXXHLXN*
V0038 NCX1000N00001NN00LHLXNXXHLXN*
V0039 NCX0100N00001NN00LHLXNXXHLXN*
V0040 NCX0010N00001NN00LHLXNXXHLXN*
V0041 NCX0001N00011NN00LHLXNXXHLXN*
V0042 NCX0000N10100NN00LHLXNXXHLXN*
V0043 NCX0000N01101NN11LHLXNXXHLXN*
V0044 NCX0000N00110NN00HLLXNXXLHXN*
V0045 NCX0000N00000NN00HLLXNXXLHXN*
C7A2B*
□F2B9

Appendix D

Avoiding Magnetic Field Interference

This appendix explains magnetic field interference issues as they relate to the FTT-10A and includes a discussion of different ways to manage interference.

Interference and Transformer-Based Transceivers

As stated in Chapter 2, *Electrical Interface*, all transformer-based transceivers—like the FTT-10A—are vulnerable to stray magnetic fields that interfere with their transformer coupling mechanism. In most environments, stray magnetic field noise is not a concern for FTT-10A transceivers. However, high frequency external magnetic fields can couple sufficient energy into the FTT-10A transceiver to cause erratic network performance or, in some cases, cause all data traffic to cease.

The FTT-10A transceiver is least sensitive to vertical stray magnetic fields and most sensitive to horizontal stray magnetic fields (i.e., fields which are parallel to the PCB on which transceiver is mounted.) Sources of stray magnetic field noise should be kept as far away from the FTT-10A transceiver as possible, and any avoidable stray magnetic fields should be oriented vertically with respect to the transceiver.

One possible source of stray magnetic fields is a DC-DC switching power supply, or regulator, using unshielded switching inductors located in close proximity to the FTT-10A transceiver. In order to minimize magnetic coupling into the FTT-10A, the switching magnetics of power supplies should be kept at least 7.5cm (3 inches) from the FTT-10A transceiver. Otherwise, noise induced into the FTT-10A receiver may affect communications.

If magnetic field interference is suspected, the level of noise at the FTT-10A should be measured. The noise induced by a switching power supply can be measured by using an oscilloscope with differential probes having at least 5V common-mode range with 50dB of common-mode rejection to measure the voltage between FTT-10A pins T1 and T2 during an interval when there is no packet activity. The noise between T1 and T2 should be less than 15mV peak-to-peak differential. In the case of noise that is magnetically coupled from a switching power supply, the noise will be synchronous with the power supply switching frequency. The worst case occurs when the coupled noise is between 10kHz and 300kHz, the center of the network data communication band. If the noise is greater than 15mV peak-to-peak, then steps should be taken to reduce the coupling effect. The easiest solution is to provide more distance between the FTT-10A transceiver and the power supply. If magnetic noise is suspected, the source can be identified by moving the suspected source away from the FTT-10A by connecting it to ≈15cm twisted pair wires and monitoring the noise at T1 and T2.

For noisy power converters, shielded inductors can provide a solution to magnetic field interference. In the commonly used "buck" style DC-DC converter, a shielded inductor can be used instead of an open-slug inductor to significantly lower the amount of stray magnetic field generated by the DC-DC converter. For example, Taiyo Yuden's LHFP-series inductor can be used instead of their LHL-series, and TDK's FS-series inductor can be used instead of their EL or ELF-series. In transformer-based DC-DC converters, the power supply designer should take care to choose a transformer style that generates minimum external stray magnetic fields. For example, a pot-core DC-DC transformer will generally produce less stray magnetic field than will an E-E core transformer, and the stray fields that it does generate are vertical when they go through the plane of the PC board. A common way to minimize magnetic fields emitted from power supply transformers is to wrap a "shorted-turn" of copper tape around the transformer in the same direction as the transformer winding.

In addition to power supplies, other noise sources can include DC motor controllers and industrial ovens/heaters. For all of these noise sources, shielding the emitting device(s) is often the most effective approach to solving magnetic field interference problems.

A magnetic shield may be necessary in environments where high ambient magnetic fields cannot be avoided. This is especially true when the base frequency of the interfering source is near or within the range of 10kHz to 300 kHz, since this range is used for communication signaling by the FTT-10A. While it is usually more effective to shield the source of the noise, as stated above, in some cases it may not be possible, sufficient, or cost- effective to shield the noise source. In such cases, the Model 51001 Magnetic Shield can be used to decrease the susceptibility of the FTT-10A to stray magnetic fields.

The Model 51001 Magnetic Shield (figure D.1) is a two-piece shield that minimizes the effects of magnetic field noise on the FTT-10A transceiver. The inner shield is mounted directly over the FTT-10A that is usually mounted on a PCB. A small amount on non-critical adhesive, such as RTV, may be used on the interior surface of the shield to fasten the shield securely to the FTT-10A plastic shell. The outer shield is then mounted in a similar way over the outside of the inner shield, forming a nested structure. It is important to remember that both materials used in the shields are electrically conductive and that the shields not be in contact with the PCB. A clearance of 0.020 to 0.040 inches should be provided to prevent possible ESD damage.

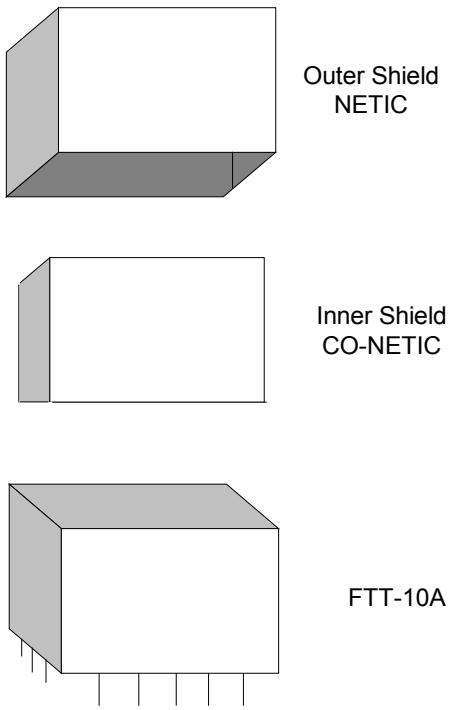


Figure D.1 FTT-10A Transceiver Magnetic Shield

Appendix E

Qualified FT/TP-10 Cable Specifications and Sources

This appendix documents two generic cable specifications that have been qualified by Echelon to work with TP/FT-10 networks. Specific vendors and their cables are cited to highlight the variety of cable types available that meet these generic specifications.

Three Qualified Cables

Echelon has qualified three cables that are available from a large number of different vendors:

(1) TIA568A Category 5 cable (24AWG/0.51mm) is widely available, and can also be found as part of structured cabling systems such as Lucent's Systimax®.

(2) NEMA Level IV cable (22 AWG/0.65mm) is available with a broad range of options, including stranded or solid, 1 or 2 pairs per cable, shielded or unshielded, and plenum or PVC.

(3) Echelon also has qualified a 16AWG/1.33mm cable. While several vendors are listed below as examples, system designers or installers can purchase cables from the vendor of their choosing provided that the cables meet the specifications outlined below.

A list of cable vendors can be found in the *Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks* engineering bulletin (005-0023-01). This document is available from Echelon's web site at www.echelon.com.

Category 5 Cable Specifications

The specification for the Telecommunications Industry Association's Commercial Building Telecommunications Cabling Standard (ANSI/TIA/EIA-568-A-95) is available from Global Engineering Documents (http://global.his.com).

NEMA Level IV Cable Specifications

The Level IV cable specification used by Echelon and as originally defined by the National Electrical Manufacturers Association (NEMA) differs from the Category IV specification proposed by the Electronic Industries Association/Telecommunication Industry Association (EIA/TIA). The Level IV cable specifications used by Echelon are presented below, and are followed by a list of Level IV cable suppliers.

Specifications apply to shielded or unshielded 22AWG (0.65mm) cable, 24AWG (0.5mm) cable shown in brackets [ ] if different	
D-C Resistance (Ohms/1000 feet at 20°C) maximum for a single copper conductor regardless of whether it is solid or stranded and is or is not metal-coated.	18.0 [28.6]
D-C Resistance Unbalance (percent) maximum	5
Mutual Capacitance of a Pair (pF/foot) maximum	17
Pair-to-Ground Capacitance Unbalance (pF/1000 feet) maximum	1000

Impedance (Ohms)	
772kHz	102±15% (87-117)
1.0MHz	100±15% (85-115)
4.0MHz	100±15% (85-115)
8.0MHz	100±15% (85-115)
10.0MHz	100±15% (85-115)
16.0MHz	100±15% (85-115)
20.0MHz	100±15% (85-115)

Attenuation (dB/1000 feet at 20°C) maximum	
772kHz	4.5 [5.7]
1.0MHz	5.5 [6.5]
4.0MHz	11.0 [13.0]
8.0MHz	15.0 [19.0]
10.0MHz	17.0 [22.0]
16.0MHz	22.0 [27.0]
20.0MHz	24.0 [31.0]
Worst-Pair Near-End Crosstalk (dB) minimum. Values are shown for information only. The minimum NEXT coupling loss for any pair combination at room temperature is to be greater than the value determined using the formula NEXT (F_{MHz})>NEXT(0.772)-15$\log_{10}$(F_{MHz}/0.772) for all frequencies in the range of 0.772MHz-20MHz for a length of 1000 feet.	
772kHz	58
1.0MHz	56
4.0MHz	47
8.0MHz	42
10.0MHz	41
16.0MHz	38
20.0MHz	36

16AWG/1.3mm "Generic" Cable Specifications

The specifications for the 16AWG/1.3mm "Generic" cable qualified by Echelon for use with TP/FT-10 networks is presented below. The generic single twisted pair is stranded (19 x 29) with tinned copper.

	Minimum	Typical	Maximum	Units	Condition
DC-Resistance, each conductor	14.0	14.7	15.5	Ω/km	20°C per ASTM D 4566
D-C Resistance Unbalance			5%		20°C per ASTM D 4566
Mutual Capacitance			55.9	nF/km	Per ASTM D 4566
Characteristic Impedance	92	100	108	Ω	64kHz to 1MHz, per ASTM D 4566

	Minimum	Typical	Maximum	Units	Condition
Attenuation				dB/km	20°C per ASTM D 4566
20kHz			1.3		
64kHz			1.9		
78kHz			2.2		
156kHz			3.0		
256kHz			4.8		
512kHz			8.1		
772kHz			11.3		
1000kHz			13.7		
Propagation Delay			5.6	ns/m	78kHz

Appendix F

FTT-10A Network Isolation Choke Specifications

This appendix provides a schematic, specifications and supplier information for the FTT-10A Network Isolation Common-Mode Choke.

FTT-10A Network Isolation Common-Mode Choke Schematic and Footprint

Below are the schematic symbol and a representative footprint for the FTT-10A Network Isolation Choke. This common-mode choke can be used to significantly increase the immunity of the FTT-10A transceiver to EN 61000-4-6 testing. It also provides significant insertion loss for common-mode RF signals up to about 500MHz, so it may provide additional margin for radiated EMI compliance. (This footprint for the FTT-10A Network Isolation Choke matches the footprint of the muRata PLT1R53C common-mode high-frequency EMI choke recommended in chapter 5.)

The Network Isolation Choke can be used in place of the EMI choke. When substituting the Network Isolation Choke for the EMI choke, the node must be re-tested for radiated EMI compliance.

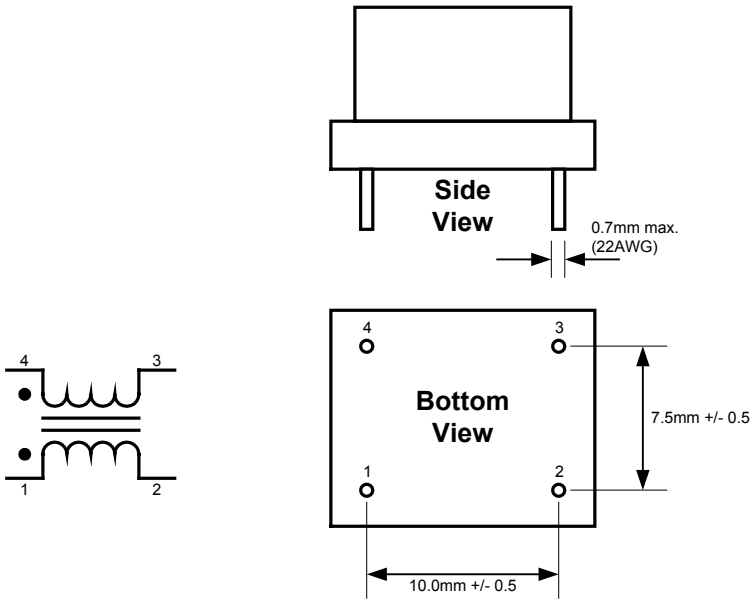


Figure F.1 Schematic Drawing and Representative Mechanical Dimensions of Choke

This common-mode isolation choke is wired in line with the network twisted pair cabling either near the node or directly on the PCB adjacent to the FTT-10A transceiver. When the choke is placed on the PCB, it will typically be located between the spark gaps and the rest of the transceiver circuit, as shown in the following figure.

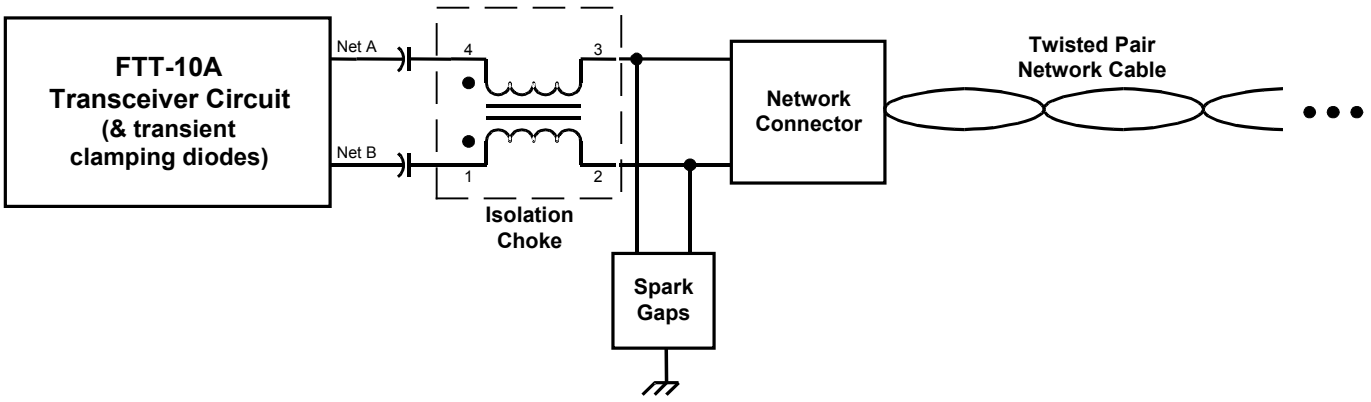


Figure F.2 Typical Placement of Network Isolation Choke in Transceiver Circuit

FTT-10A Network Isolation Choke Specifications

Below are the electrical specifications for the FTT-10A Network Isolation Choke. These specifications must be met over the full operating temperature range of the transceiver circuit.

Parameter (over –40C to +85C)	***Min***	***Typ***	***Max***	***Units***
Turns Ratio (1-2) : (3-4)	1:1		1:1	Turns
DC Resistance 1-2 3-4			 1.5 1.5	 Ohm Ohm
Magnetizing Inductance 1-2 10kHz, 1Vrms (3-4 open)	1.8			mH
Magnetizing Inductance 3-4 10kHz, 1Vrms (1-2 open)	1.8			mH
Leakage Inductance 1-2 10kHz, 1Vrms (3-4 shorted)			5.0	µH
Leakage Inductance 3-4 10kHz, 1Vrms (1-2 shorted)			5.0	µH
Differential Capacitance 1-4 10kHz, 1Vrms (1-2 shorted, 3-4 shorted)			40	pF
Differential Voltage Withstand 1-4 60Hz (1-2 shorted, 3-4 shorted)	500			V

Below are the material parameters and construction details for a choke that meets the electrical specifications listed in the previous table.

Parameter	***Construction Details***
Number of Turns (1-2) : (3-4)	37:37
Core Type	Ferrite Toroid
Core Size	12.7mm(OD) x 7.14mm(ID) x 4.78mm(H)
Core Magnetic Properties, Relative Permeability, Typ. @ 20C A_L, Minimum @ -40C	 5000 1.32 nH/N^2
Wire Type and Size	32 AWG solid, with extruded insulation
Wire Insulation for Low Capacitance	PTFE, Tefzel or Polypropylene
Wire Insulation Dielectric Coefficient	2.0-2.8
Wire Insulation Thickness	0.005-0.007 inches (0.13-0.18mm)
Wire Insulation Color Winding 1-2 Winding 3-4	 Green White
Bifilar Wire Winding	Wind 37 times with both wires (primary and secondary) at the same time.
Toroid Winding Technique	Wind the 37 bifilar turns in one evenly distributed layer around the full circumference of the toroid, and terminate the wires on the header pins according to the schematic in figure E.1

FTT-10A Network Isolation Choke Vendors

Contact the following vendors for details on mechanical design information, and pricing.

Vendor	*Part Number*	*Contact Instructions*
Complete Isolation Choke Assembly: Transpower Technologies, Inc. 4805 Double R Blvd., Suite 100 Reno, NV 89511	TTI7570	Telephone: +1-775-852-0140 Fax: +1-775-852-0145
Ferrite Core: Magnetics Inc. Division of Spang & Company P.O. Box 391 Butler, PA 16003	Type OJ-41407-TC	Telephone: +1-724-282-8282 +1-800-245-3984 Fax: +1-724-282-6955
Ferrite Core: TDK Cores, Distributed by: MH&W International 14 Leighton Place Mahwah, NJ 07430	Type H5B T12.4x4.77x7.14	Telephone: +1-201-891-8800 Fax: +1-201-891-0625
Ferrite Core: Steward Magnetics 1200 East 36th Street P.O. Box 510 Chattanooga, TN 37401	Type 35T0501-000	Telephone: +1-423-867-4100 +1-800-634-2673 Fax: +1-423-867-4102
Low-Capacitance Choke Wire: Whitmore/WireNetics 27737 Avenue Hopkins Valencia, CA 91355	32132-x	Telephone: +1-800-822-9473 Fax: +1-661-257-2495
4-Pin Choke Header: Lodestone Pacific 4769 Wesley Drive Anaheim, CA 92807	TM512-4	Telephone: +1-714-970-0900 Fax: +1-714-970-0800